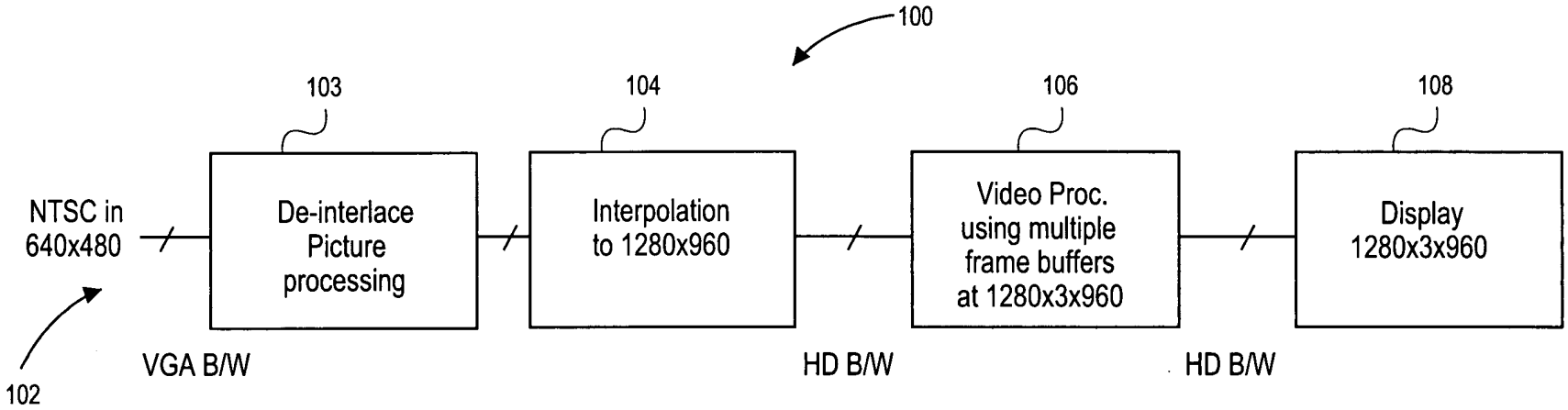


FIG. 1
(PRIOR ART)

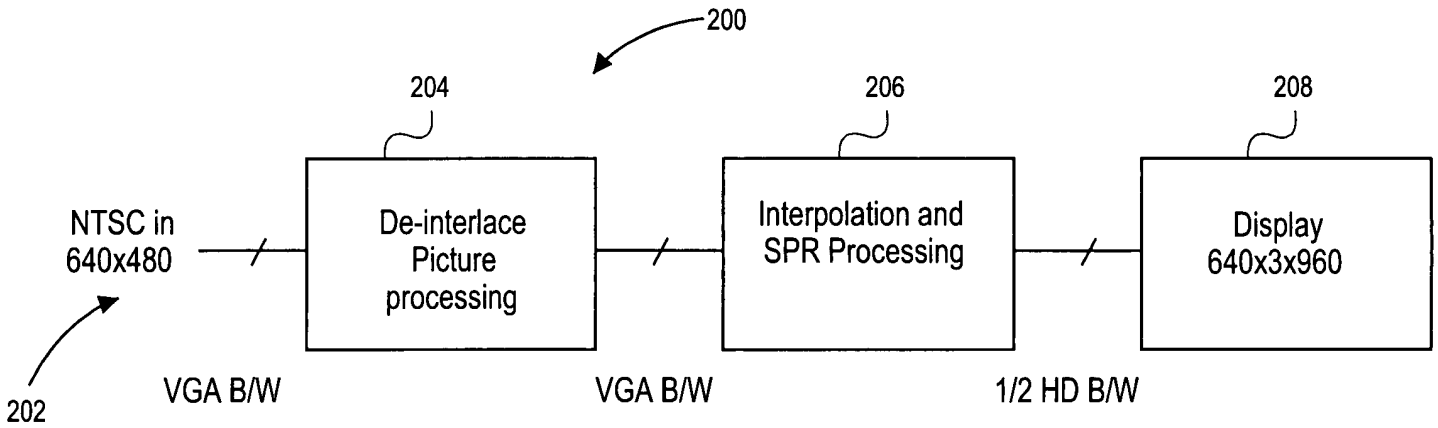


FIG. 2

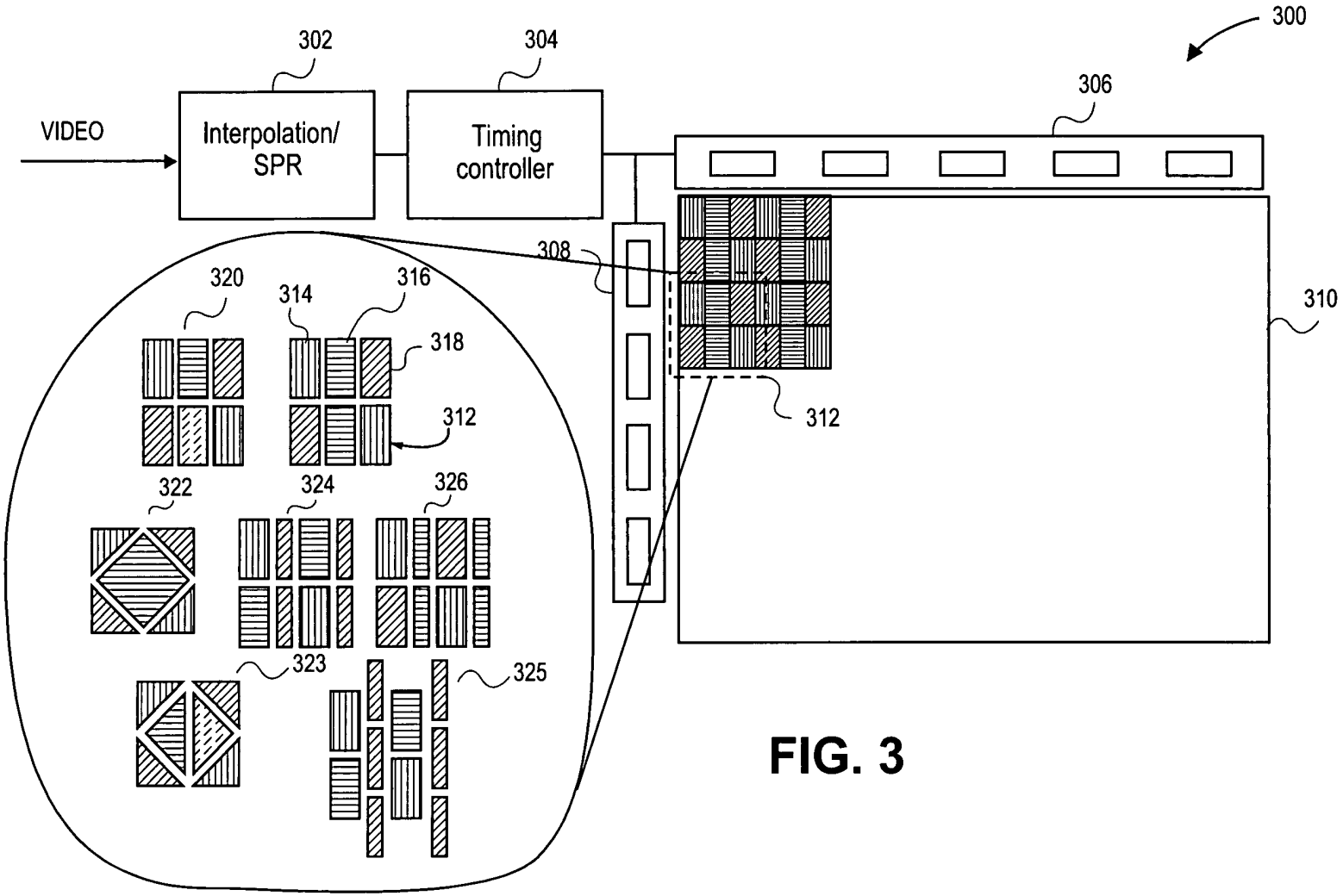

300
302
304
306
VIDEO
Interpolation/
SPR
Timing
controller
308
310
312
312
320
314
316
318
322
324
326
323
325

FIG. 3

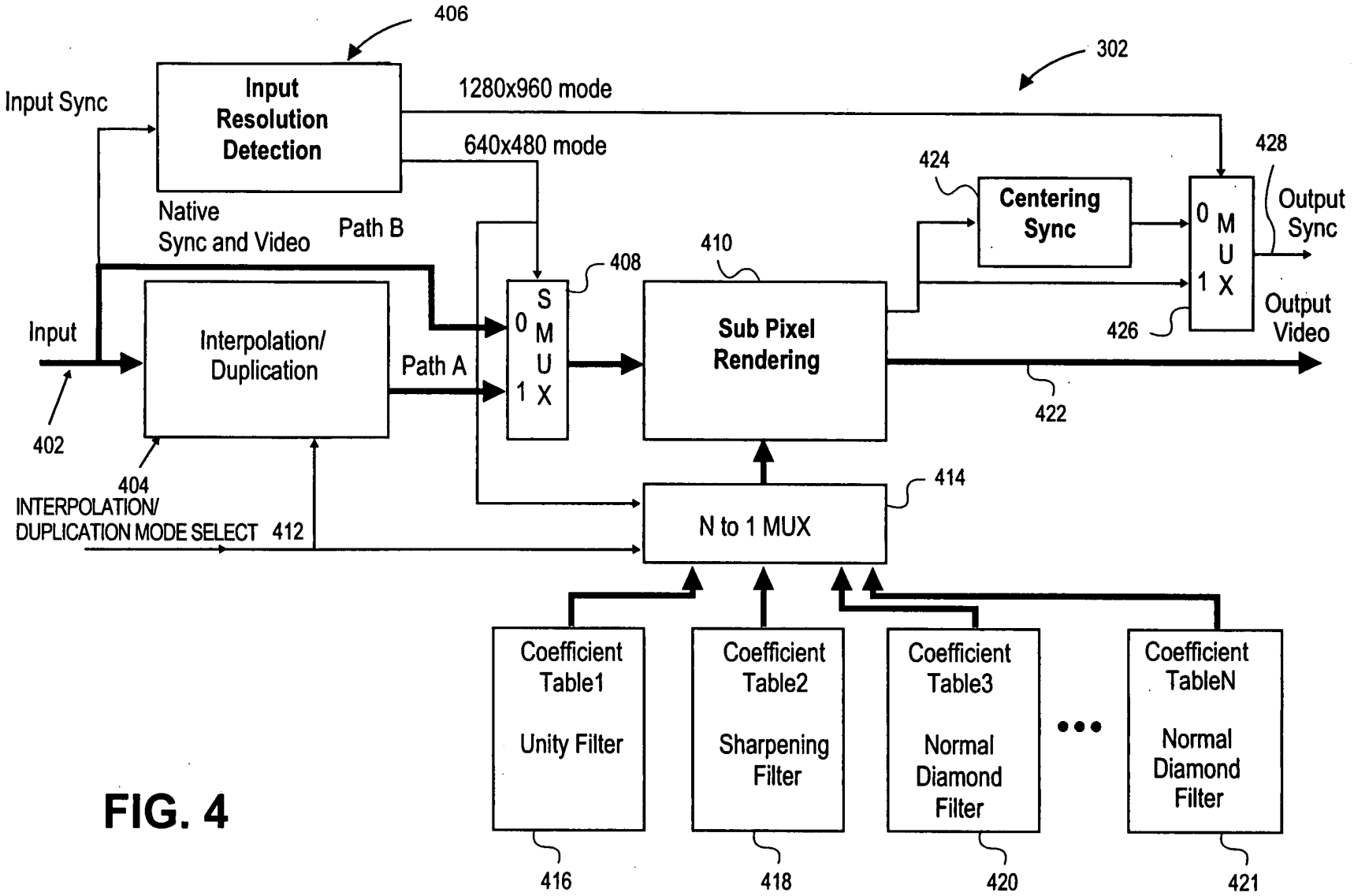

406
302
Input Sync
Input Resolution Detection
1280x960 mode
640x480 mode
428
424
Centering Sync
Output Sync
Native Sync and Video
Path B
410
408
0 MUX 1
Input
Interpolation/ Duplication
Path A
Sub Pixel Rendering
426
Output Video
422
402
404
INTERPOLATION/ DUPLICATION MODE SELECT 412
414
N to 1 MUX
Coefficient Table1
Unity Filter
Coefficient Table2
Sharpening Filter
Coefficient Table3
Normal Diamond Filter
Coefficient TableN
Normal Diamond Filter
416
418
420
421

FIG. 4

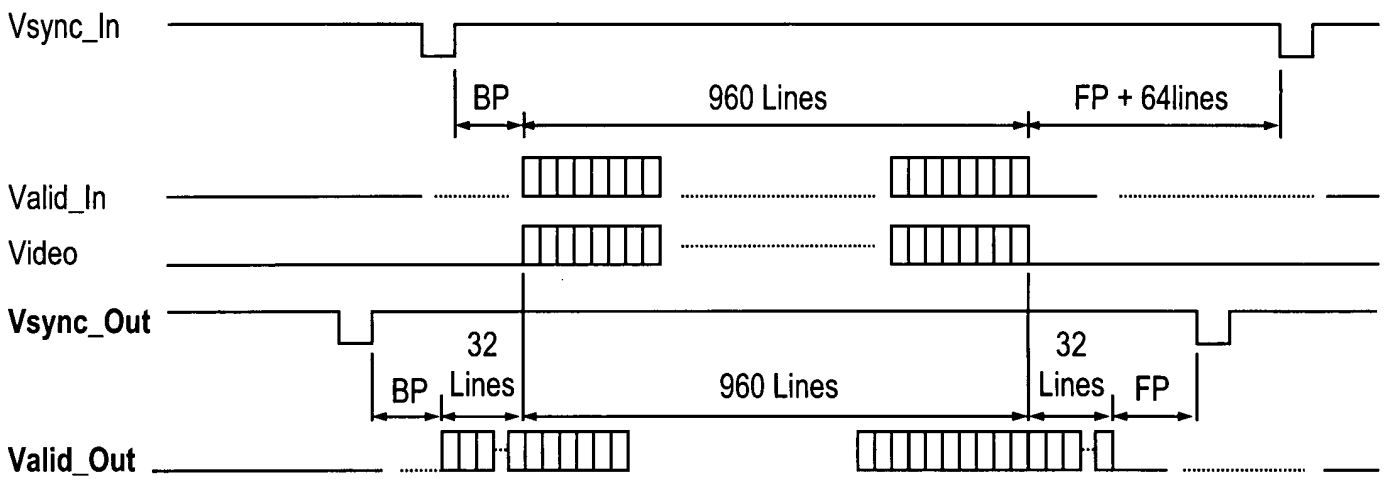

Vsync_In
BP
960 Lines
FP + 64lines
Valid_In
Video
Vsync_Out
32
Lines
BP
960 Lines
32
Lines
FP
Valid_Out

FIG. 5

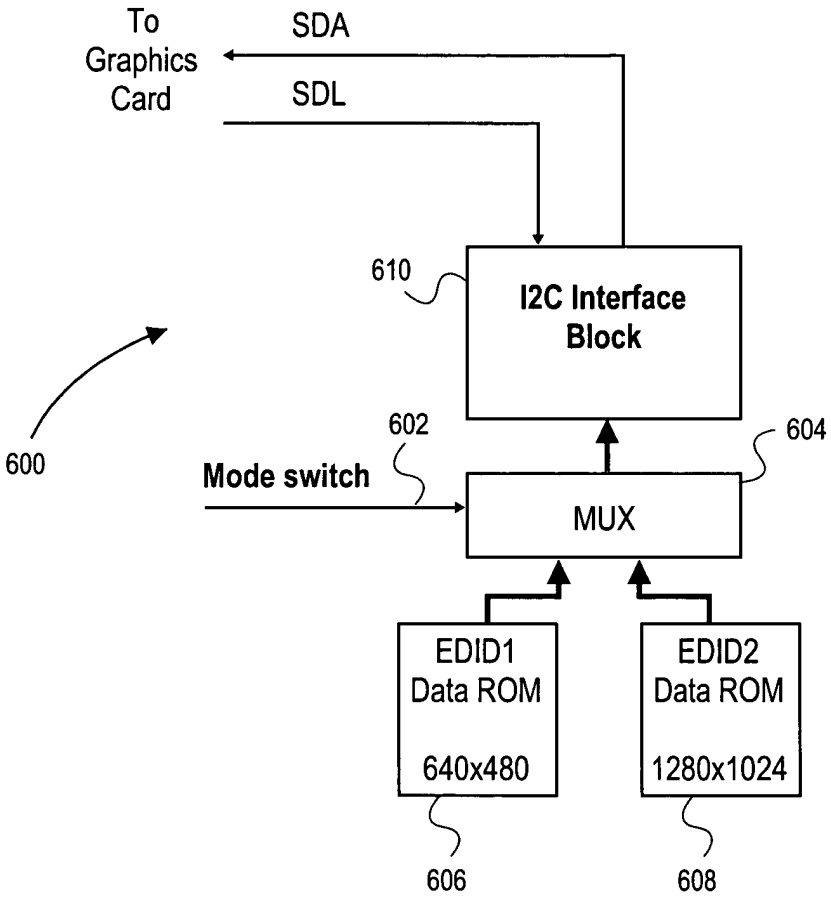

To
Graphics
Card
SDA
SDL
610
I2C Interface
Block
600
602
604
Mode switch
MUX
EDID1
Data ROM
640x480
EDID2
Data ROM
1280x1024
606
608

FIG. 6

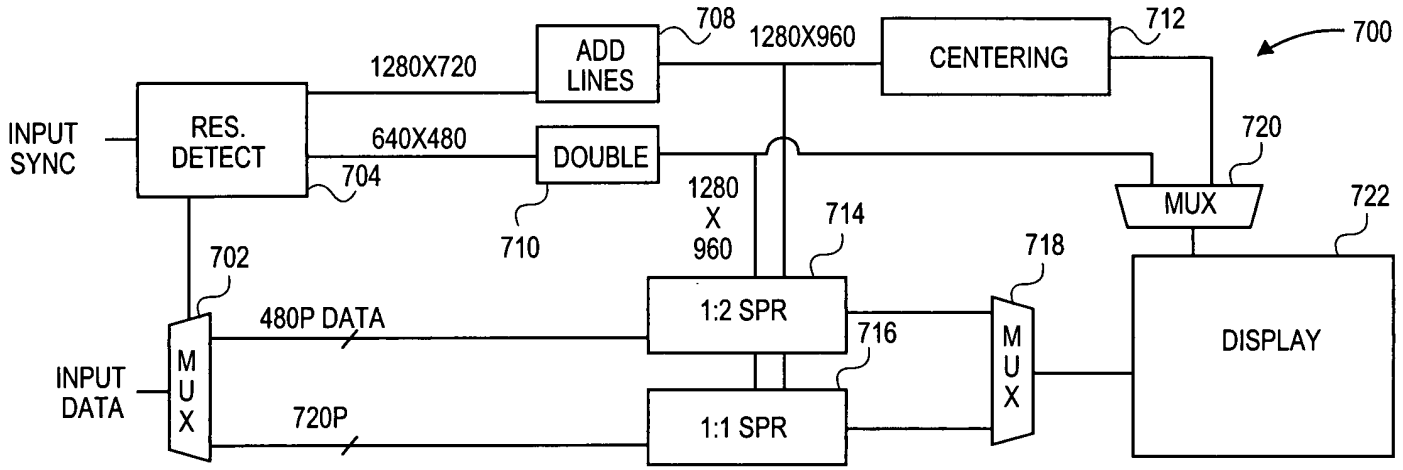

INPUT SYNC
RES. DETECT
704
1280X720
640X480
ADD LINES
DOUBLE
708
710
1280X960
1280 X 960
CENTERING
712
700
720
MUX
722
DISPLAY
714
718
702
480P DATA
1:2 SPR
716
INPUT DATA
MUX
720P
1:1 SPR
MUX

FIG. 7

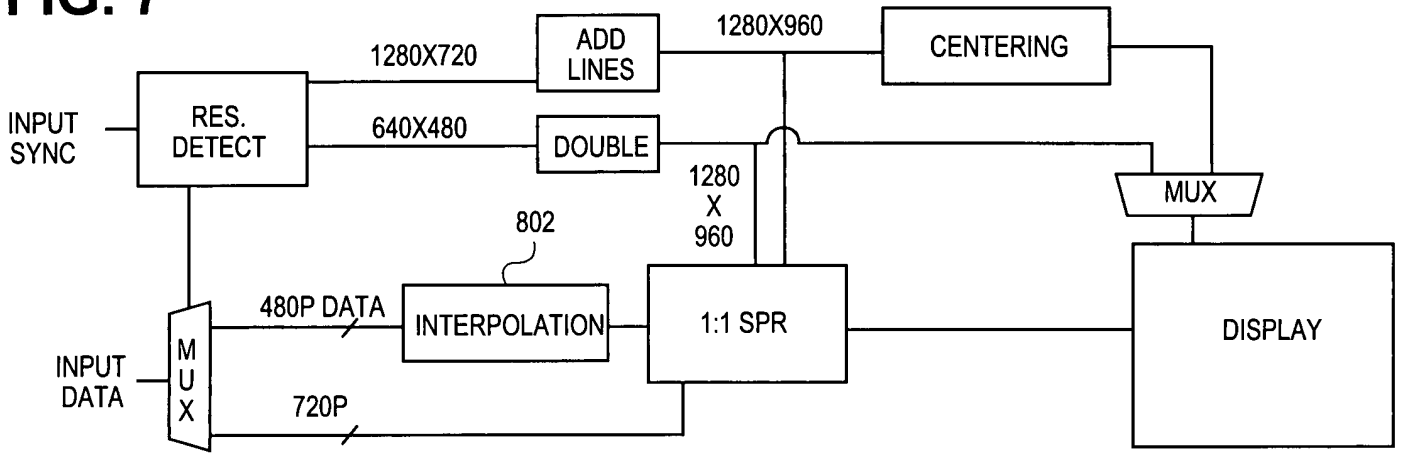

INPUT SYNC
RES. DETECT
1280X720
640X480
ADD LINES
DOUBLE
1280X960
CENTERING
MUX
1280 X 960
802
480P DATA
INTERPOLATION
1:1 SPR
DISPLAY
INPUT DATA
MUX
720P

FIG. 8

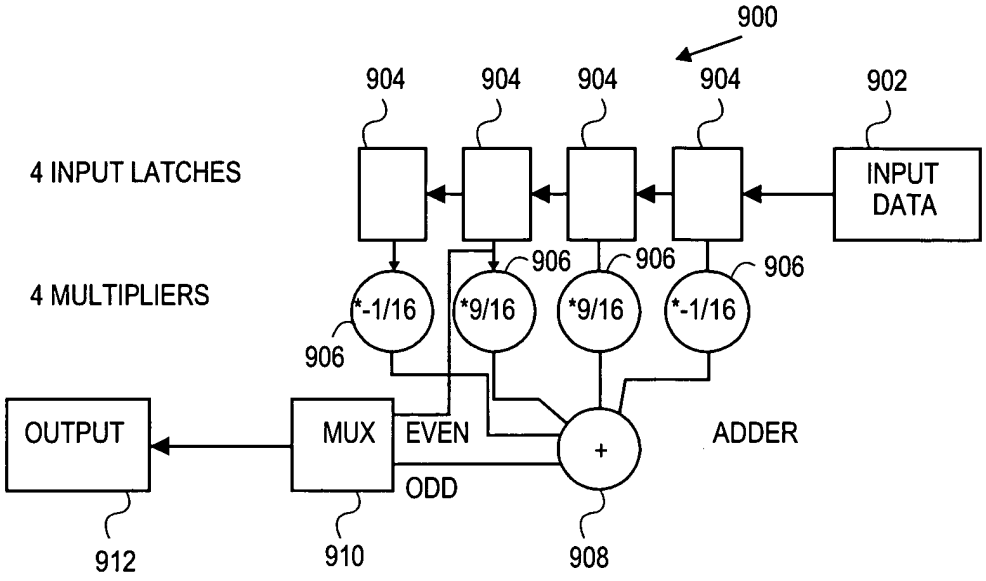

900
904
904
904
904
902
4 INPUT LATCHES
INPUT DATA
4 MULTIPLIERS
906
906
906
906
*-1/16
*9/16
*9/16
*-1/16
OUTPUT
MUX
EVEN
ODD
+
ADDER
912
910
908

FIG. 9

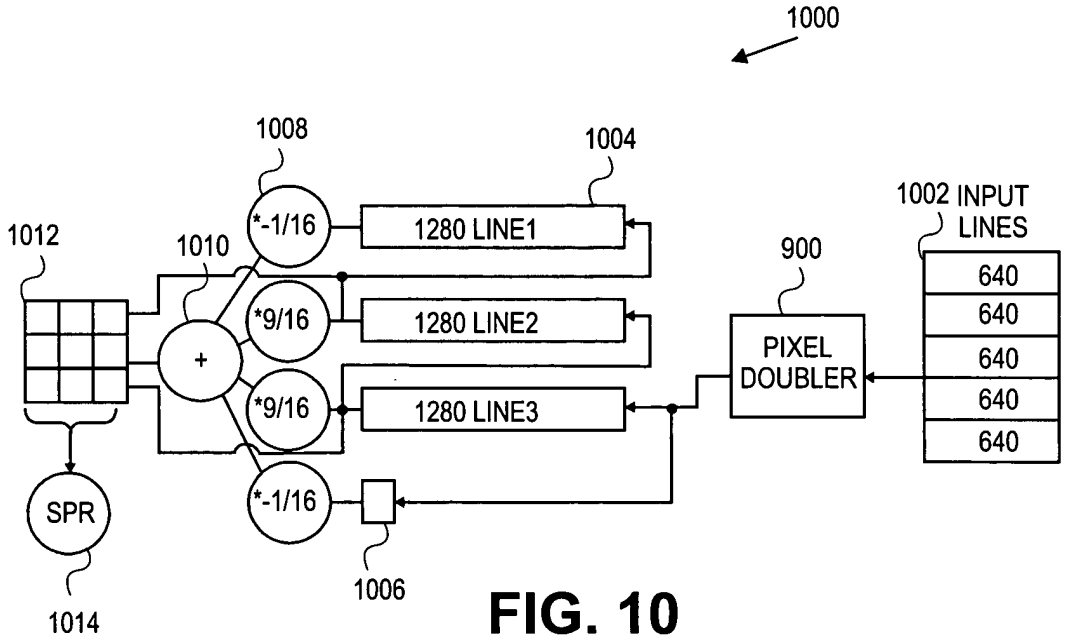

1000
1008
1004
1002 INPUT LINES
1012
1010
*-1/16
1280 LINE1
900
640
640
640
640
640
*9/16
1280 LINE2
+
PIXEL DOUBLER
*9/16
1280 LINE3
*-1/16
SPR
1006
1014

FIG. 10

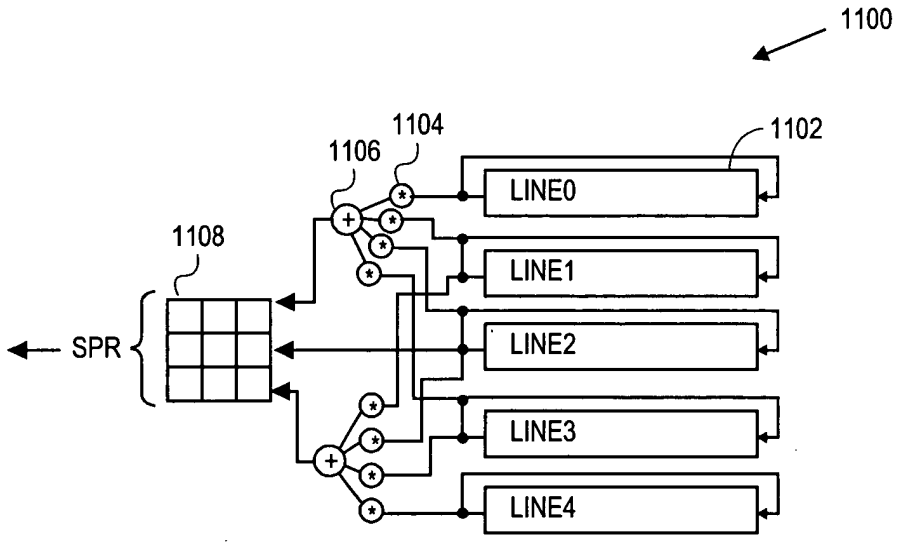

1100
1104
1106
1102
LINE0
1108
LINE1
SPR
LINE2
LINE3
LINE4

FIG. 11

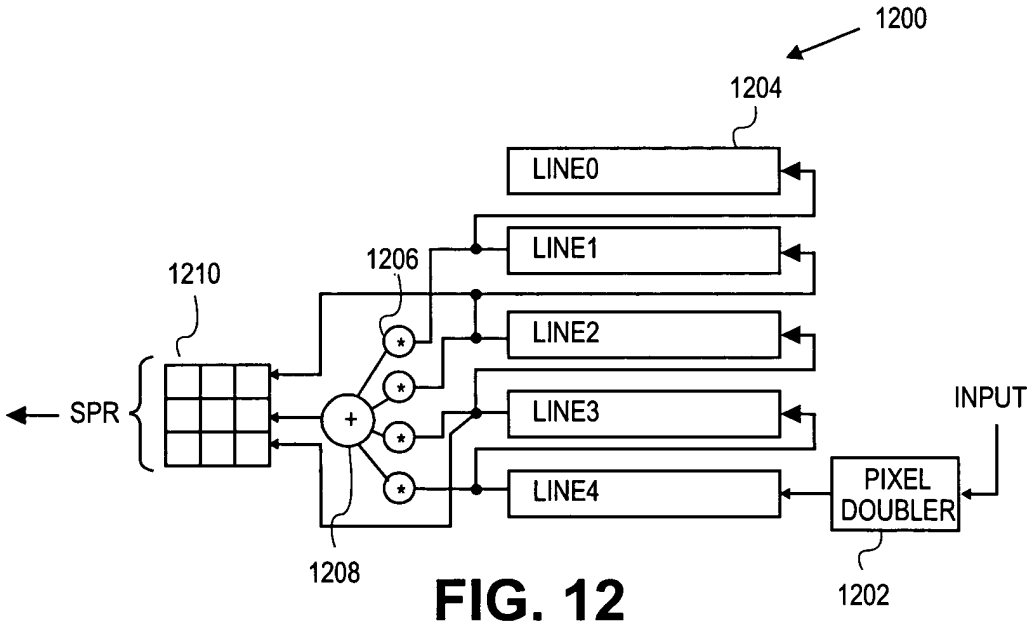

1200
1204
LINE0
LINE1
1206
1210
LINE2
SPR
LINE3
INPUT
LINE4
PIXEL DOUBLER
1208
1202

FIG. 12

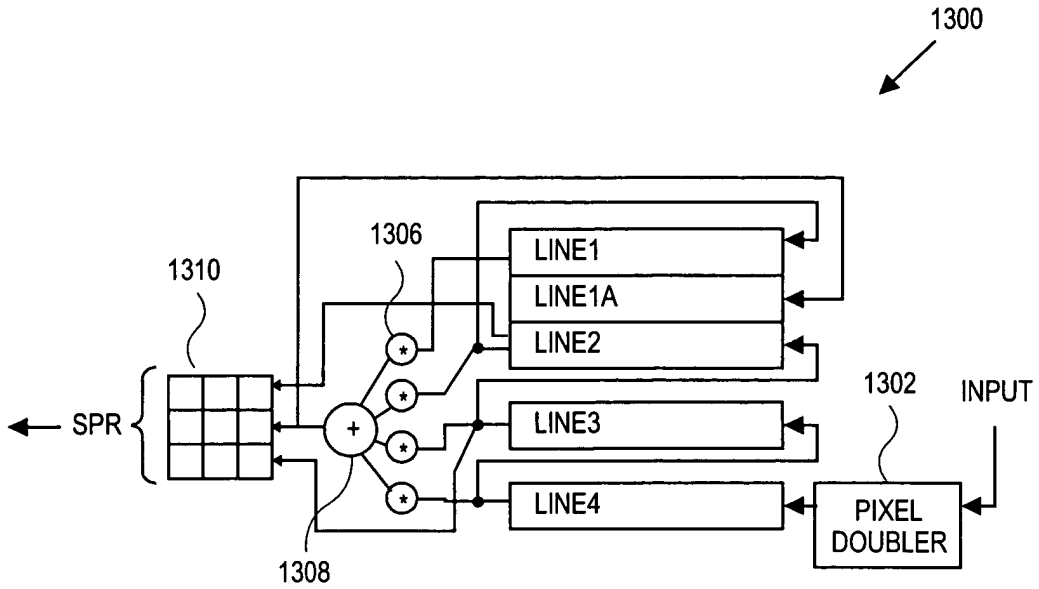

1300
1306
1310
LINE1
LINE1A
LINE2
LINE3
LINE4
1302
INPUT
SPR
PIXEL
DOUBLER
1308

FIG. 13

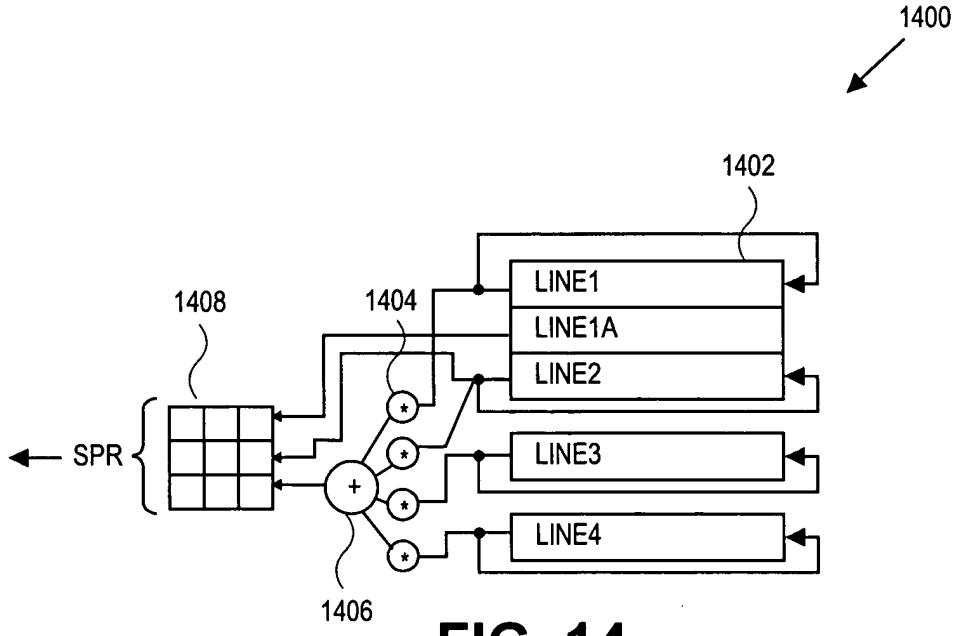

1400
1402
1408
1404
LINE1
LINE1A
LINE2
LINE3
LINE4
SPR
1406

FIG. 14

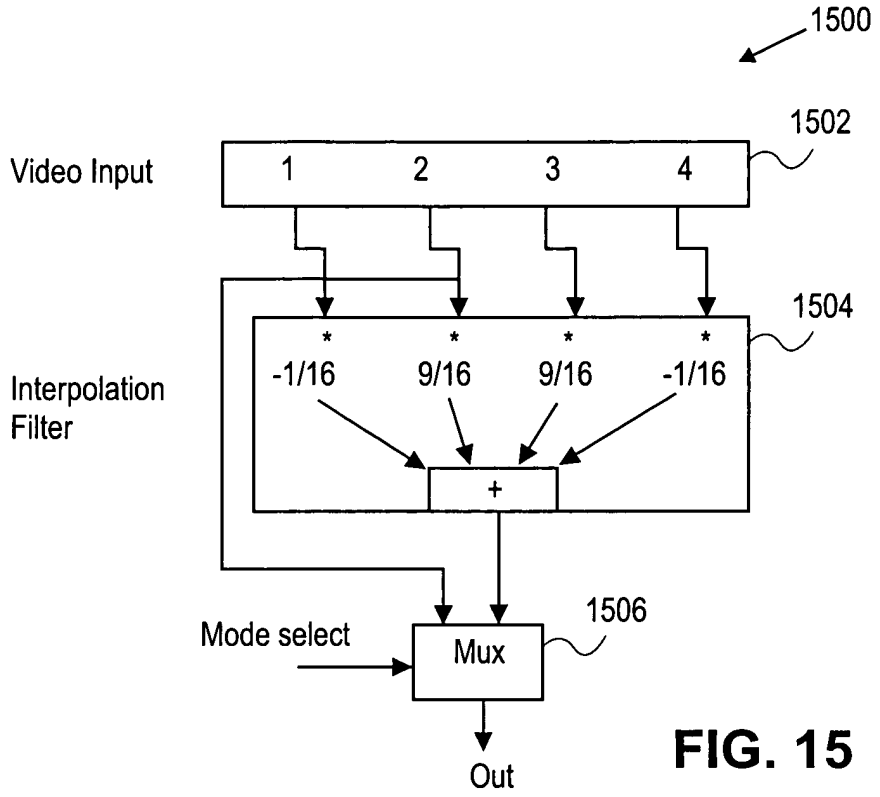


FIG. 15

Interpolation mode	1	I1	2	I2	3	I3	4	I4	5	I5
Duplication mode	1	1	2	2	3	3	4	4	5	5

FIG. 16

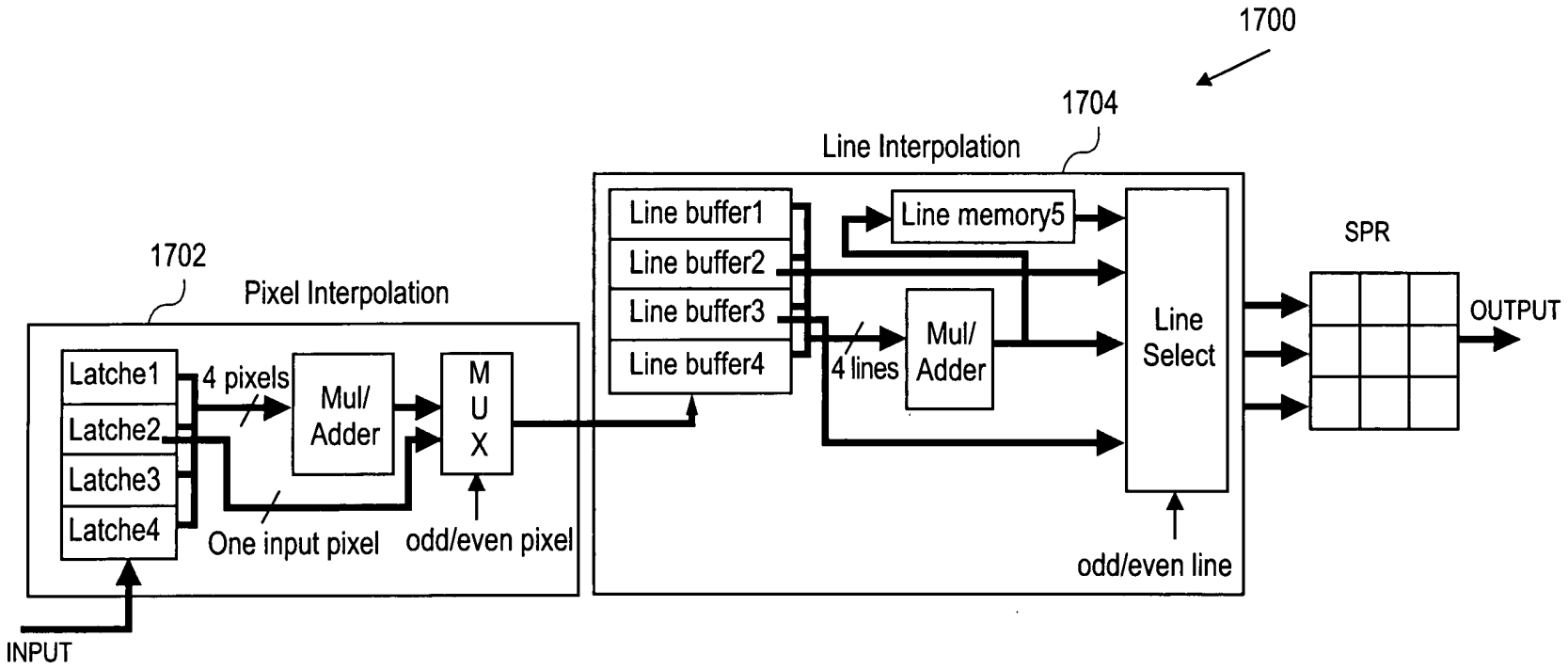

1700
1704
Line Interpolation
Line buffer1
Line buffer2
Line buffer3
Line buffer4
Line memory5
4 lines
Mul/
Adder
Line
Select
SPR
OUTPUT
odd/even line
1702
Pixel Interpolation
Latche1
Latche2
Latche3
Latche4
4 pixels
Mul/
Adder
M
U
X
One input pixel
odd/even pixel
INPUT

FIG. 17

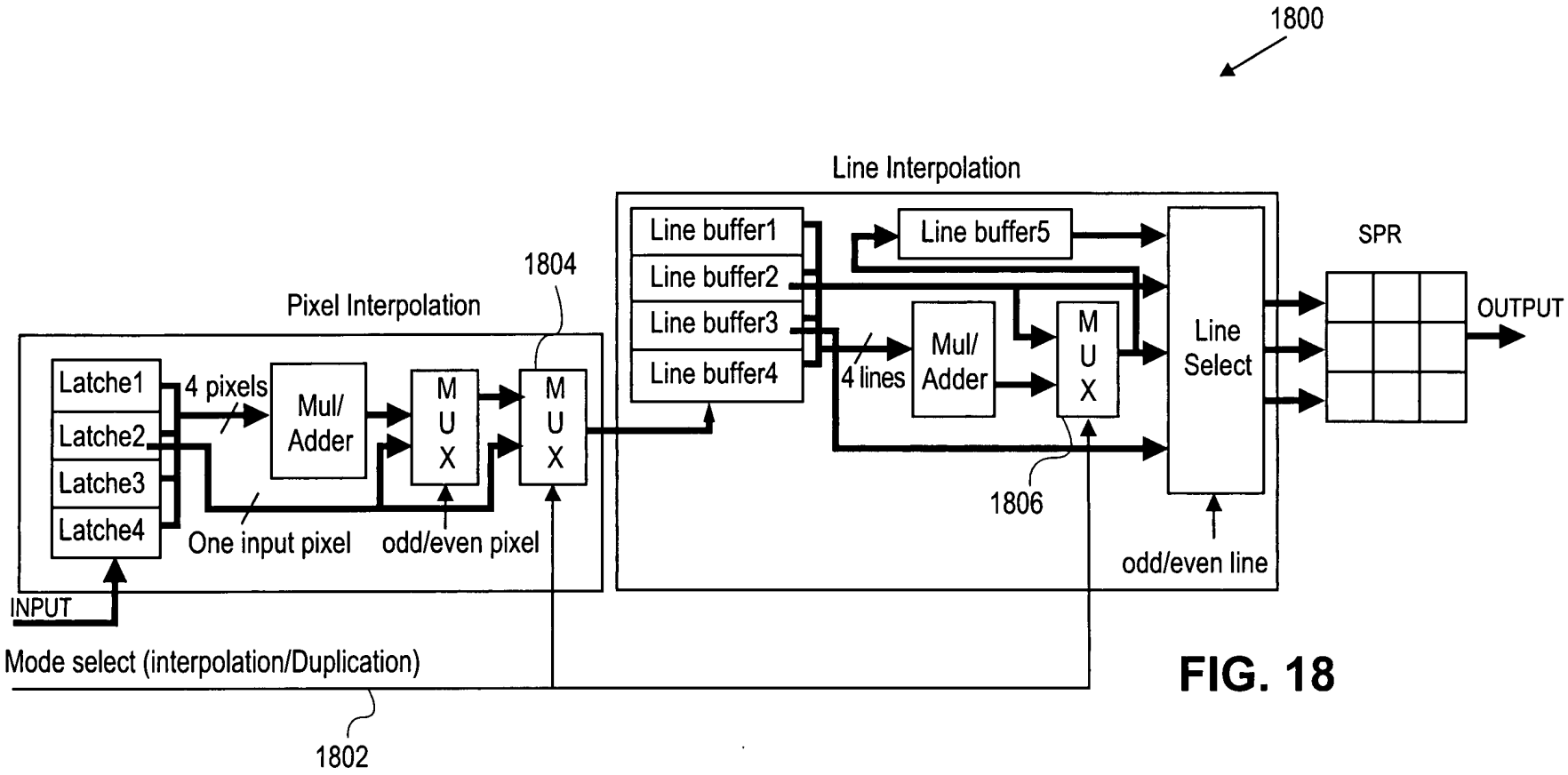

1800
Line Interpolation
Line buffer1
Line buffer2
Line buffer3
Line buffer4
Line buffer5
SPR
OUTPUT
1804
Pixel Interpolation
Latche1
Latche2
Latche3
Latche4
4 pixels
Mul/
Adder
M
U
X
M
U
X
4 lines
Mul/
Adder
M
U
X
Line
Select
One input pixel
odd/even pixel
1806
odd/even line
INPUT
Mode select (interpolation/Duplication)
1802

FIG. 18

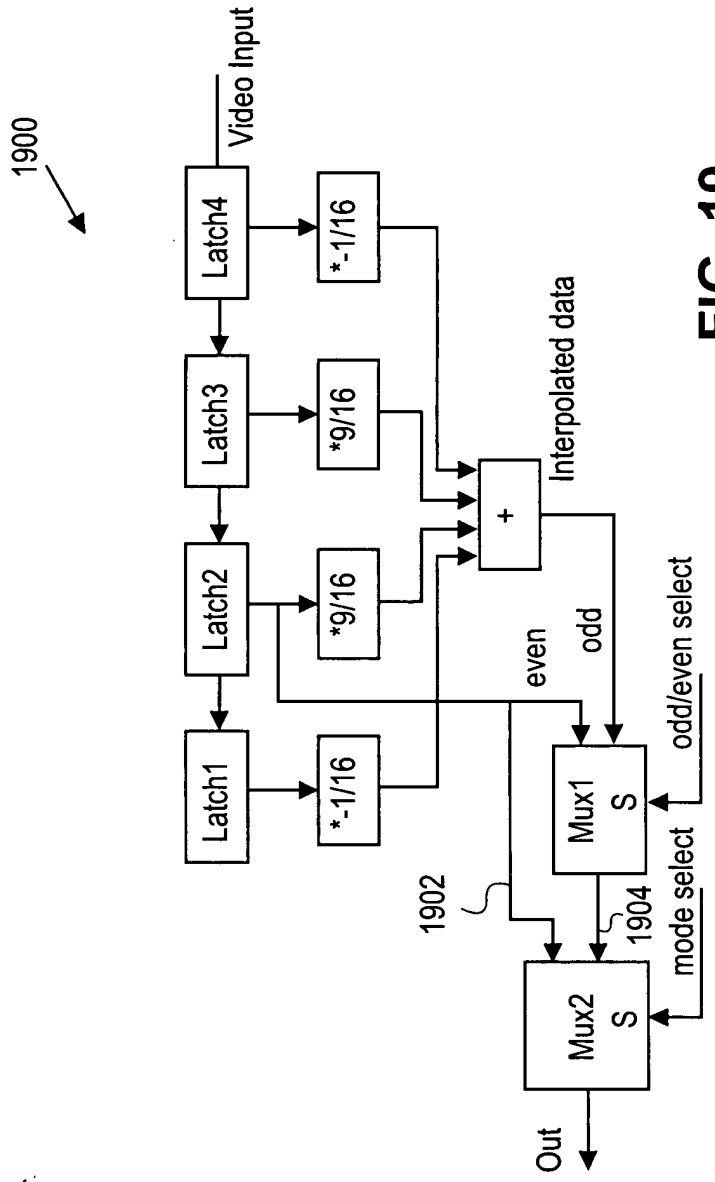

1900
Video Input
Latch4
Latch3
Latch2
Latch1
*-1/16
*9/16
*9/16
*-1/16
+
Interpolated data
even
odd
1902
1904
Mux1
S
odd/even select
Mux2
S
mode select
Out

FIG. 19

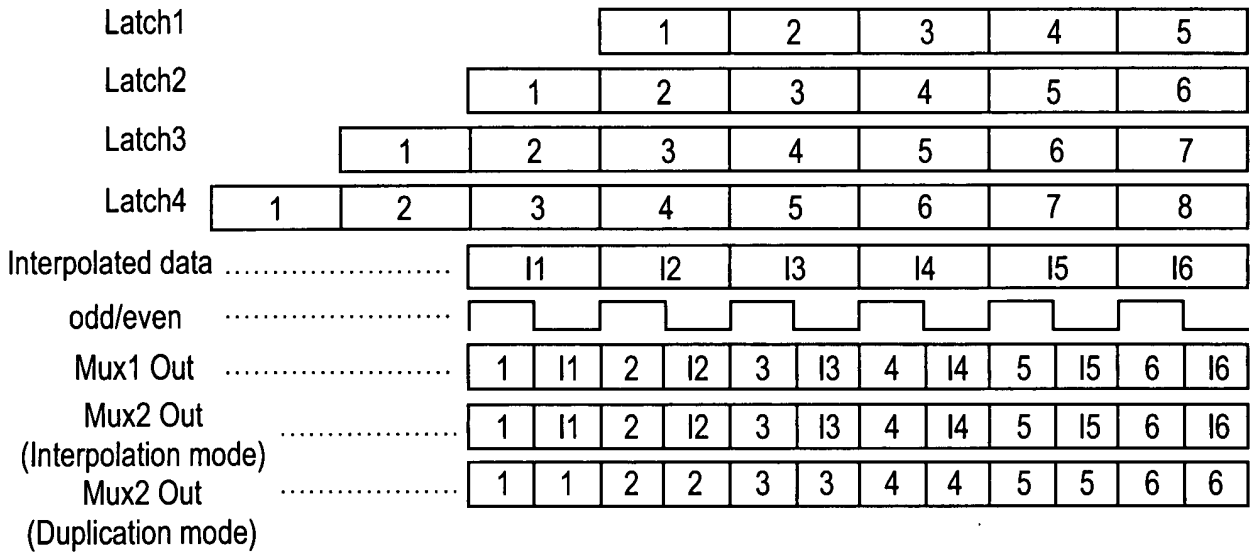

Latch1
Latch2
Latch3
Latch4
Interpolated data
odd/even
Mux1 Out
Mux2 Out
(Interpolation mode)
Mux2 Out
(Duplication mode)
1 2 3 4 5 6 7 8
I1 I2 I3 I4 I5 I6

FIG. 20

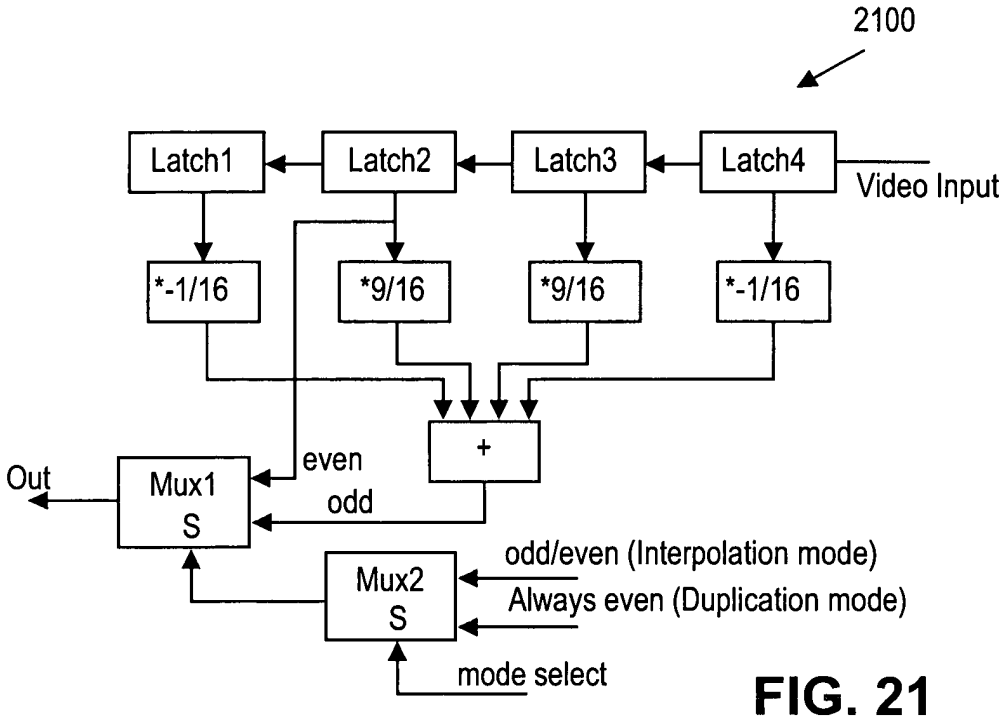

2100
Latch1
Latch2
Latch3
Latch4
Video Input
*-1/16
*9/16
*9/16
*-1/16
+
Out
Mux1
S
even
odd
Mux2
S
odd/even (Interpolation mode)
Always even (Duplication mode)
mode select

FIG. 21

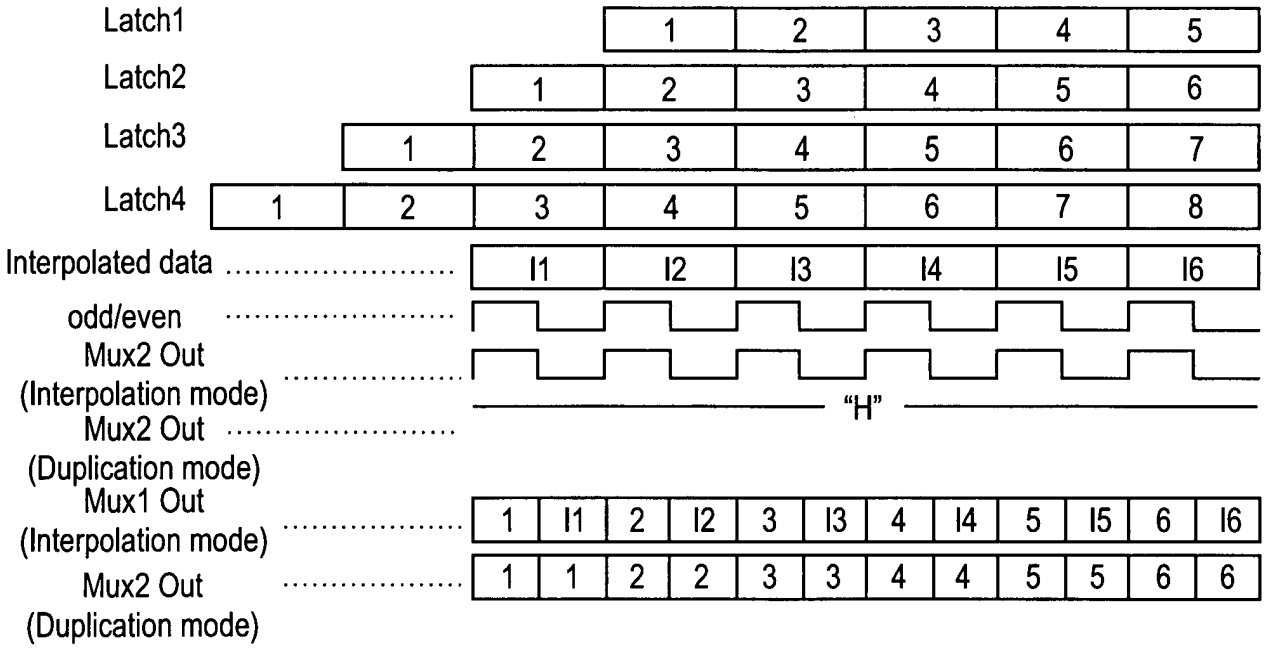

Latch1
Latch2
Latch3
Latch4
Interpolated data
odd/even
Mux2 Out
(Interpolation mode)
Mux2 Out
(Duplication mode)
Mux1 Out
(Interpolation mode)
Mux2 Out
(Duplication mode)
"H"

FIG. 22

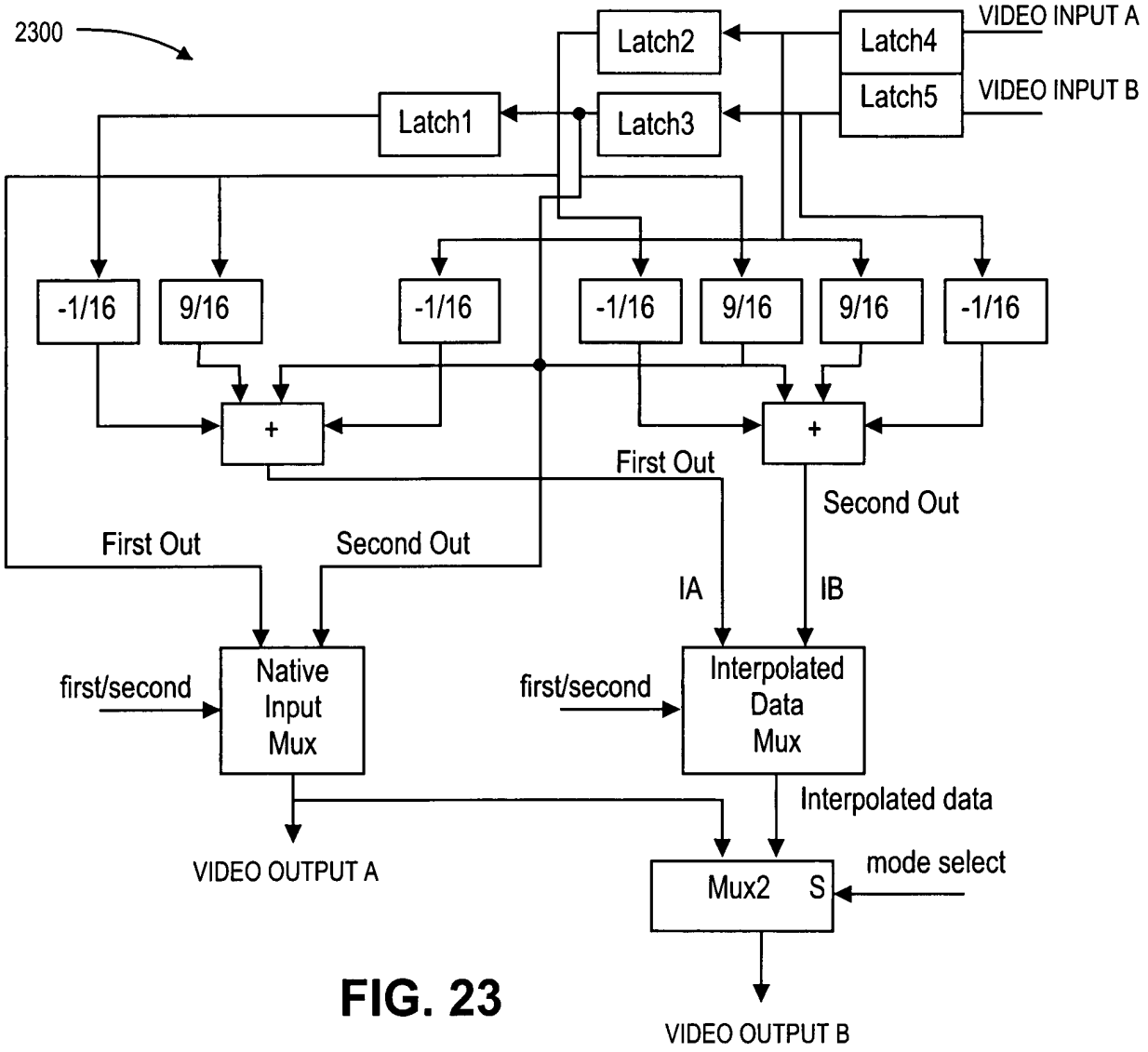

2300
Latch2
Latch4
VIDEO INPUT A
Latch5
VIDEO INPUT B
Latch1
Latch3
-1/16
9/16
-1/16
-1/16
9/16
9/16
-1/16
+
+
First Out
Second Out
First Out
Second Out
IA
IB
first/second
Native Input Mux
first/second
Interpolated Data Mux
Interpolated data
VIDEO OUTPUT A
mode select
Mux2
S
VIDEO OUTPUT B

FIG. 23

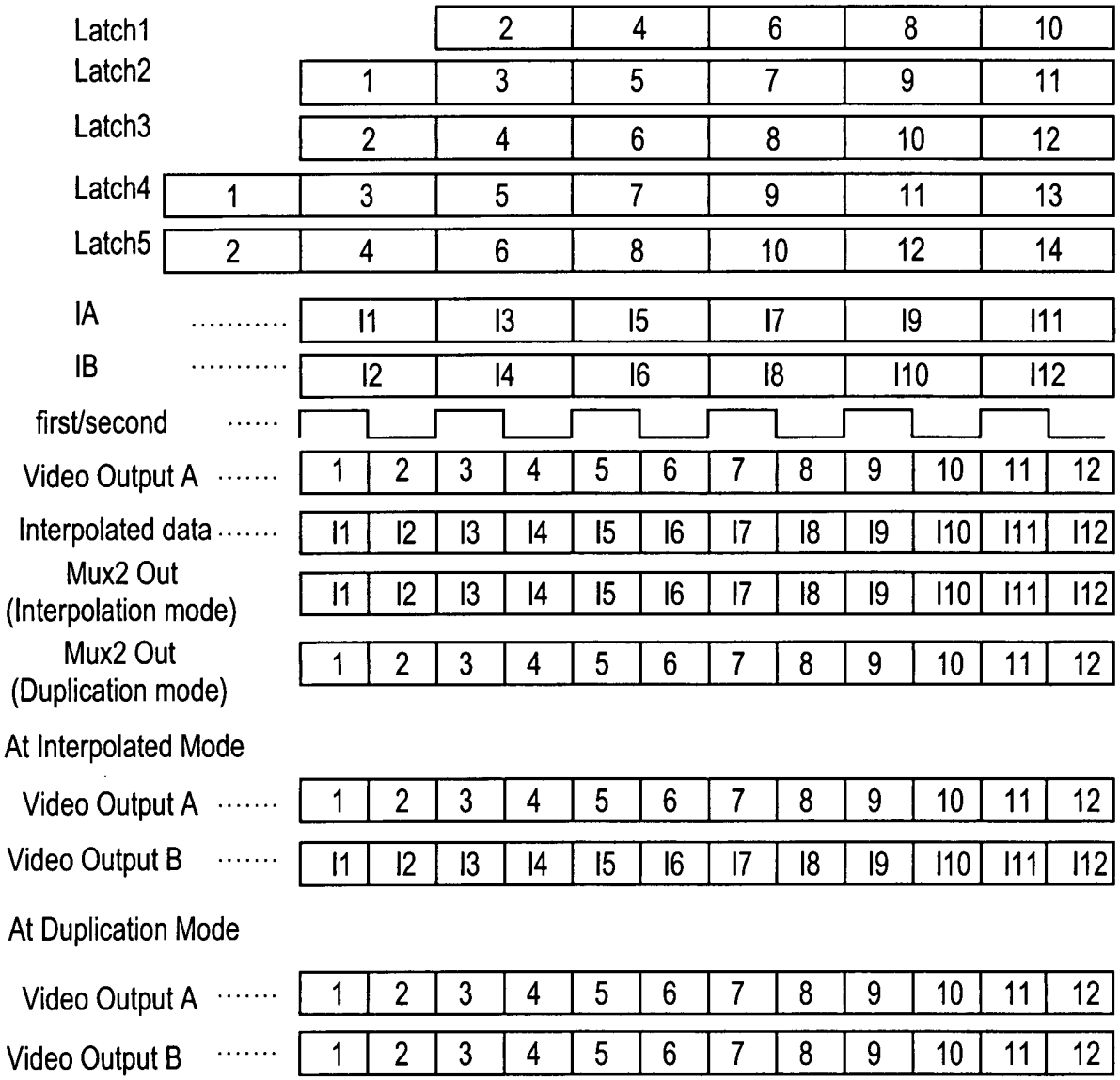

Latch1
Latch2
Latch3
Latch4
Latch5
IA
IB
first/second
Video Output A
Interpolated data
Mux2 Out (Interpolation mode)
Mux2 Out (Duplication mode)
At Interpolated Mode
Video Output A
Video Output B
At Duplication Mode
Video Output A
Video Output B

FIG. 24

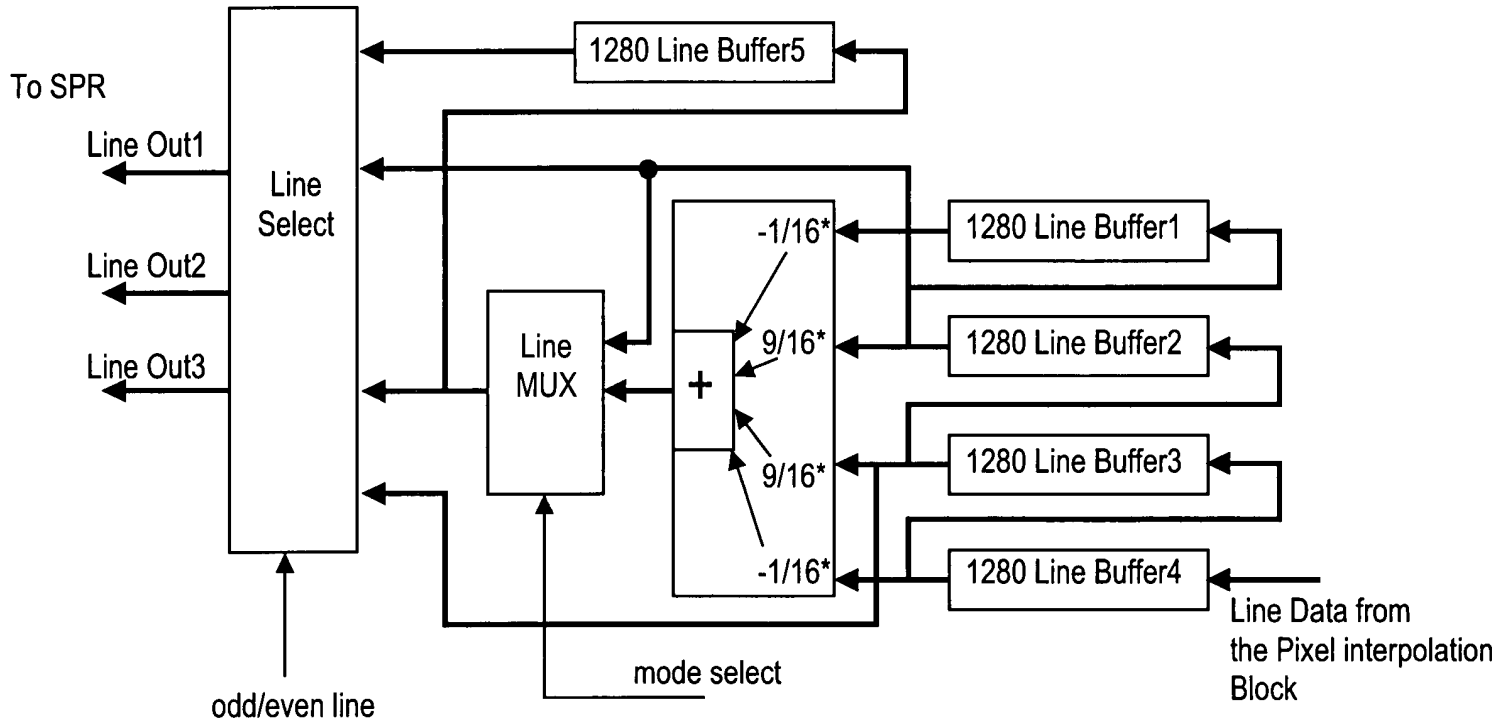

To SPR
Line Out1
Line Out2
Line Out3
Line Select
1280 Line Buffer5
1280 Line Buffer1
1280 Line Buffer2
1280 Line Buffer3
1280 Line Buffer4
-1/16*
9/16*
9/16*
-1/16*
+
Line MUX
odd/even line
mode select
Line Data from the Pixel interpolation Block

FIG. 25

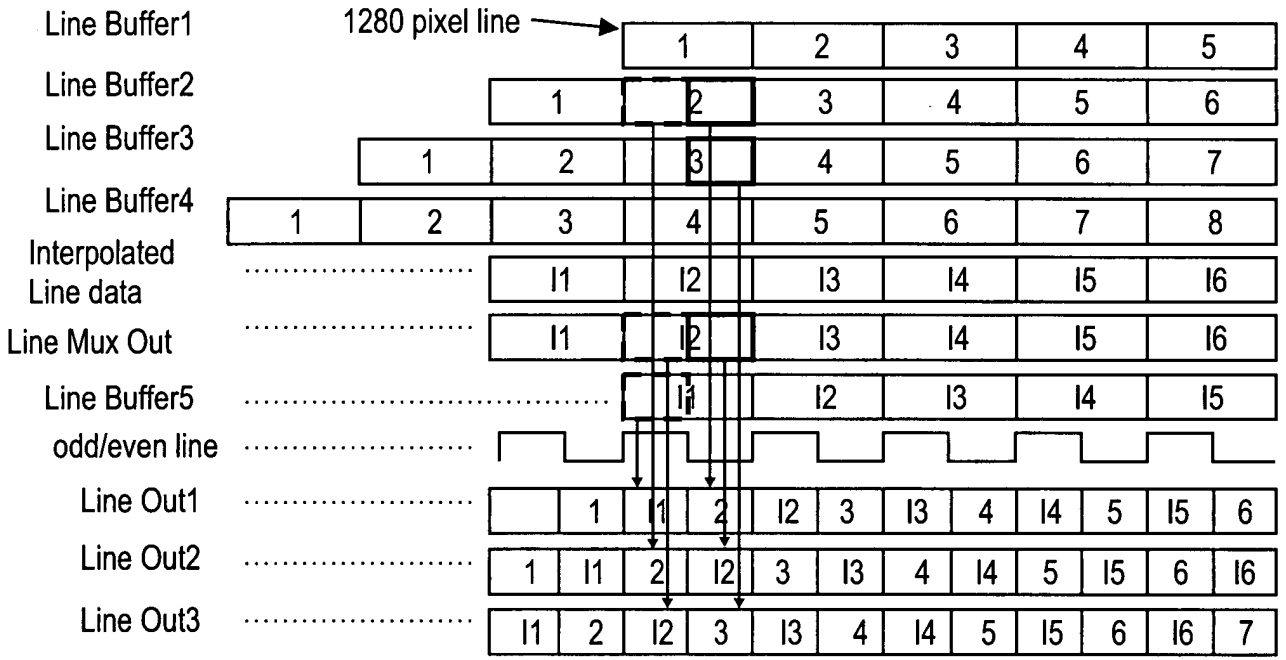

Line Buffer1
1280 pixel line
Line Buffer2
Line Buffer3
Line Buffer4
Interpolated Line data
Line Mux Out
Line Buffer5
odd/even line
Line Out1
Line Out2
Line Out3

FIG. 26

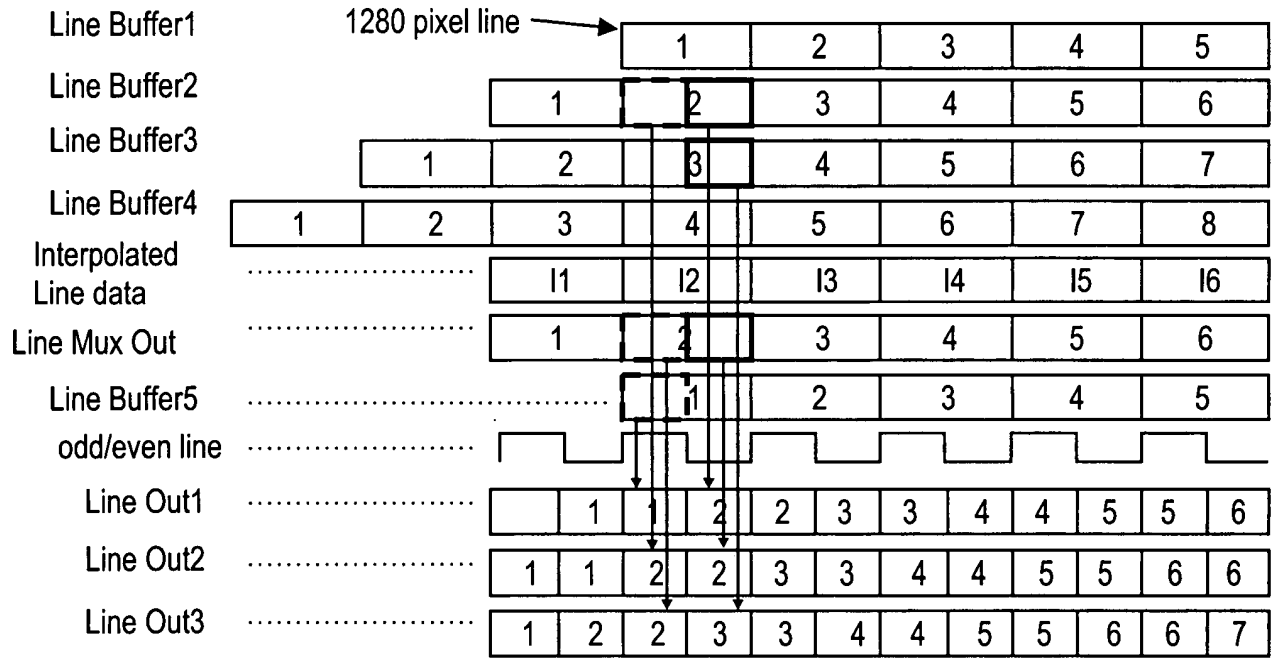

Line Buffer1
1280 pixel line
Line Buffer2
Line Buffer3
Line Buffer4
Interpolated Line data
Line Mux Out
Line Buffer5
odd/even line
Line Out1
Line Out2
Line Out3

FIG. 27

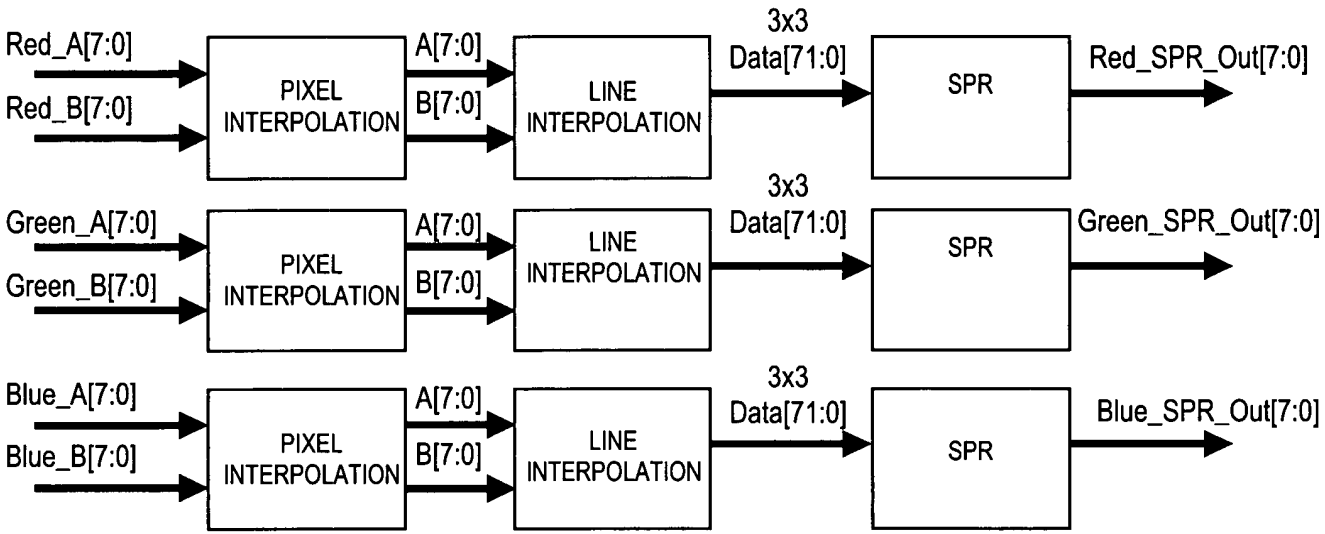

Red_A[7:0]
Red_B[7:0]
PIXEL INTERPOLATION
A[7:0]
B[7:0]
LINE INTERPOLATION
3x3 Data[71:0]
SPR
Red_SPR_Out[7:0]
Green_A[7:0]
Green_B[7:0]
PIXEL INTERPOLATION
A[7:0]
B[7:0]
LINE INTERPOLATION
3x3 Data[71:0]
SPR
Green_SPR_Out[7:0]
Blue_A[7:0]
Blue_B[7:0]
PIXEL INTERPOLATION
A[7:0]
B[7:0]
LINE INTERPOLATION
3x3 Data[71:0]
SPR
Blue_SPR_Out[7:0]

FIG. 28

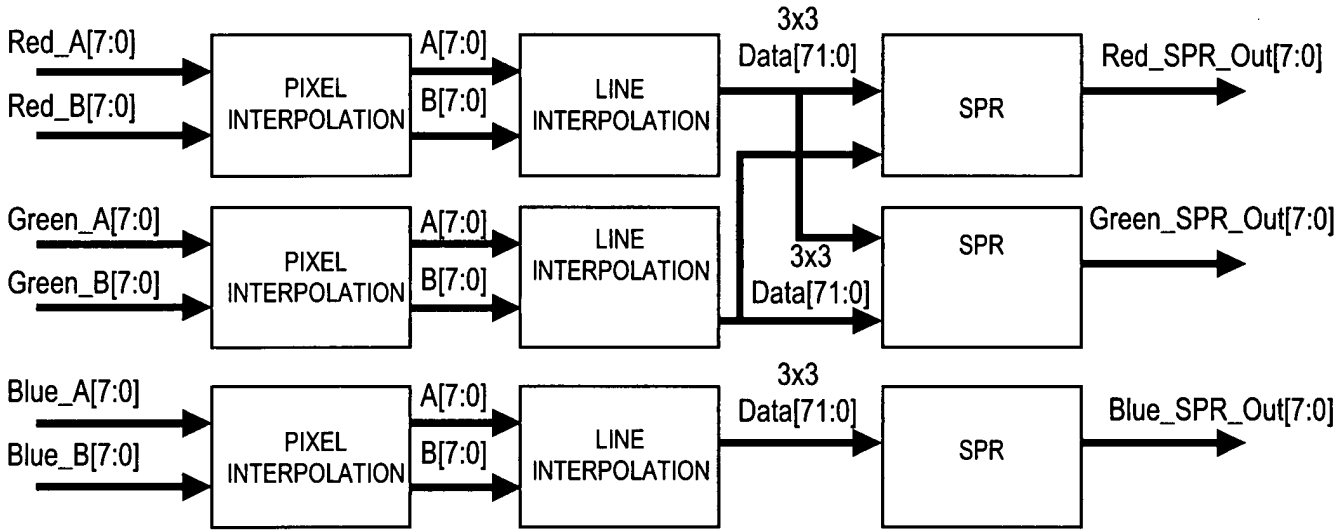

Red_A[7:0]
Red_B[7:0]
PIXEL INTERPOLATION
A[7:0]
B[7:0]
LINE INTERPOLATION
3x3 Data[71:0]
SPR
Red_SPR_Out[7:0]
Green_A[7:0]
Green_B[7:0]
PIXEL INTERPOLATION
A[7:0]
B[7:0]
LINE INTERPOLATION
3x3 Data[71:0]
SPR
Green_SPR_Out[7:0]
Blue_A[7:0]
Blue_B[7:0]
PIXEL INTERPOLATION
A[7:0]
B[7:0]
LINE INTERPOLATION
3x3 Data[71:0]
SPR
Blue_SPR_Out[7:0]

FIG. 29

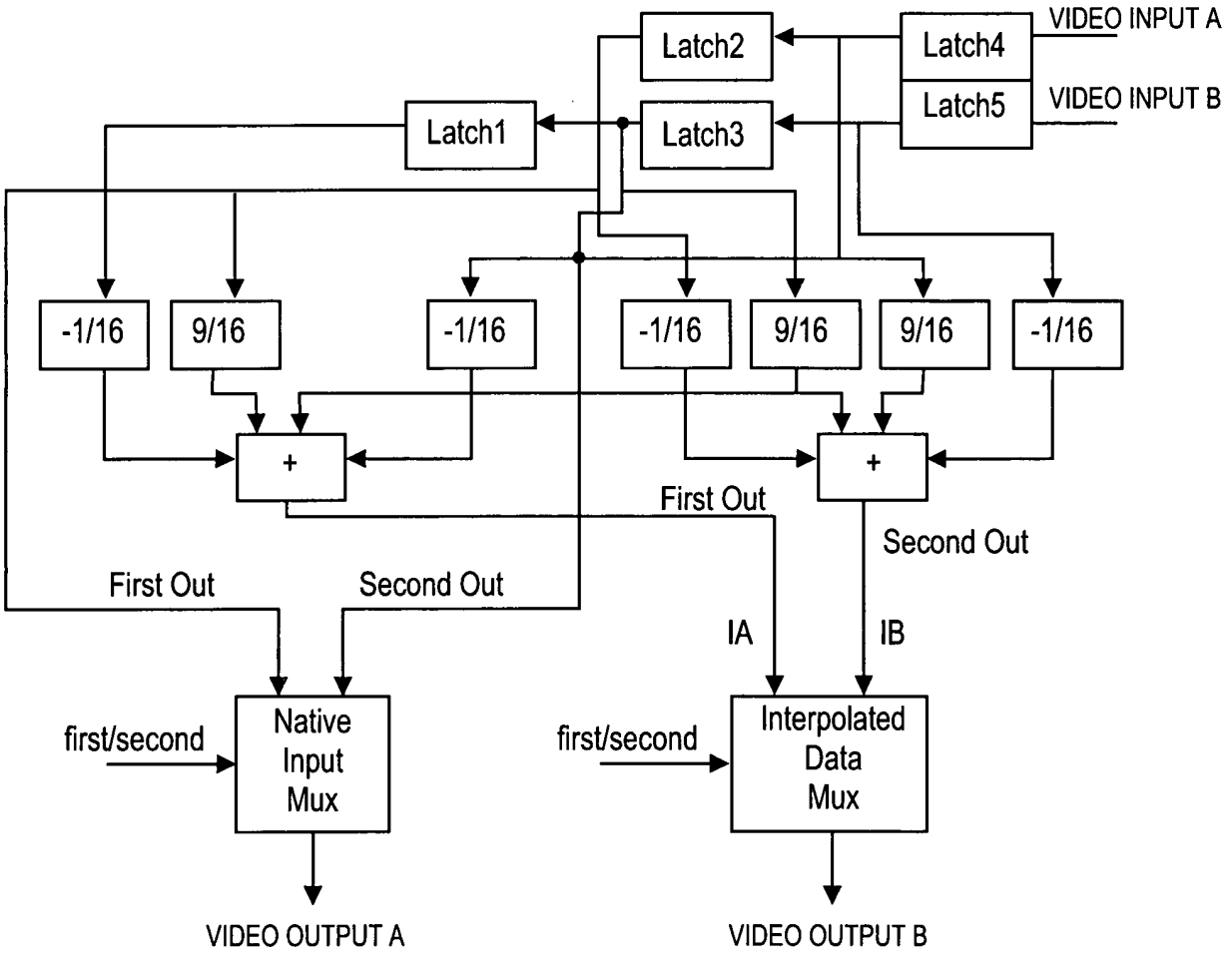
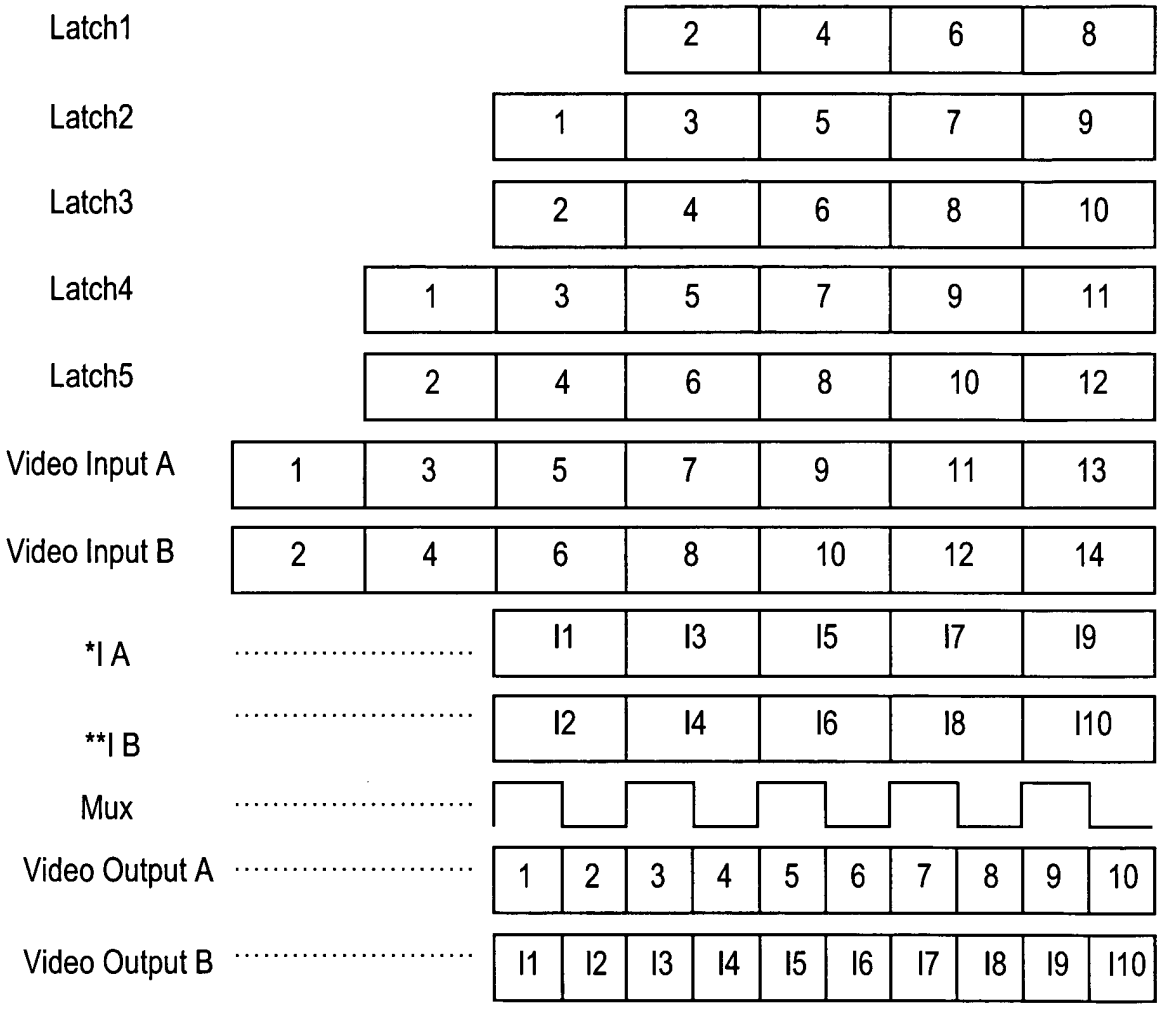

Latch2
Latch4
VIDEO INPUT A
Latch5
VIDEO INPUT B
Latch1
Latch3
-1/16
9/16
-1/16
-1/16
9/16
9/16
-1/16
+
+
First Out
Second Out
First Out
Second Out
IA
IB
first/second
Native Input Mux
first/second
Interpolated Data Mux
VIDEO OUTPUT A
VIDEO OUTPUT B

FIG. 30



* IA =Latch1*(-1/16) + Latch2*(9/16) + Latch3*(9/16) + Latch4*(-1/16)

** IB =Latch2*(-1/16) + Latch3*(9/16) + Latch4*(9/16) + Latch5*(-1/16)

FIG. 31

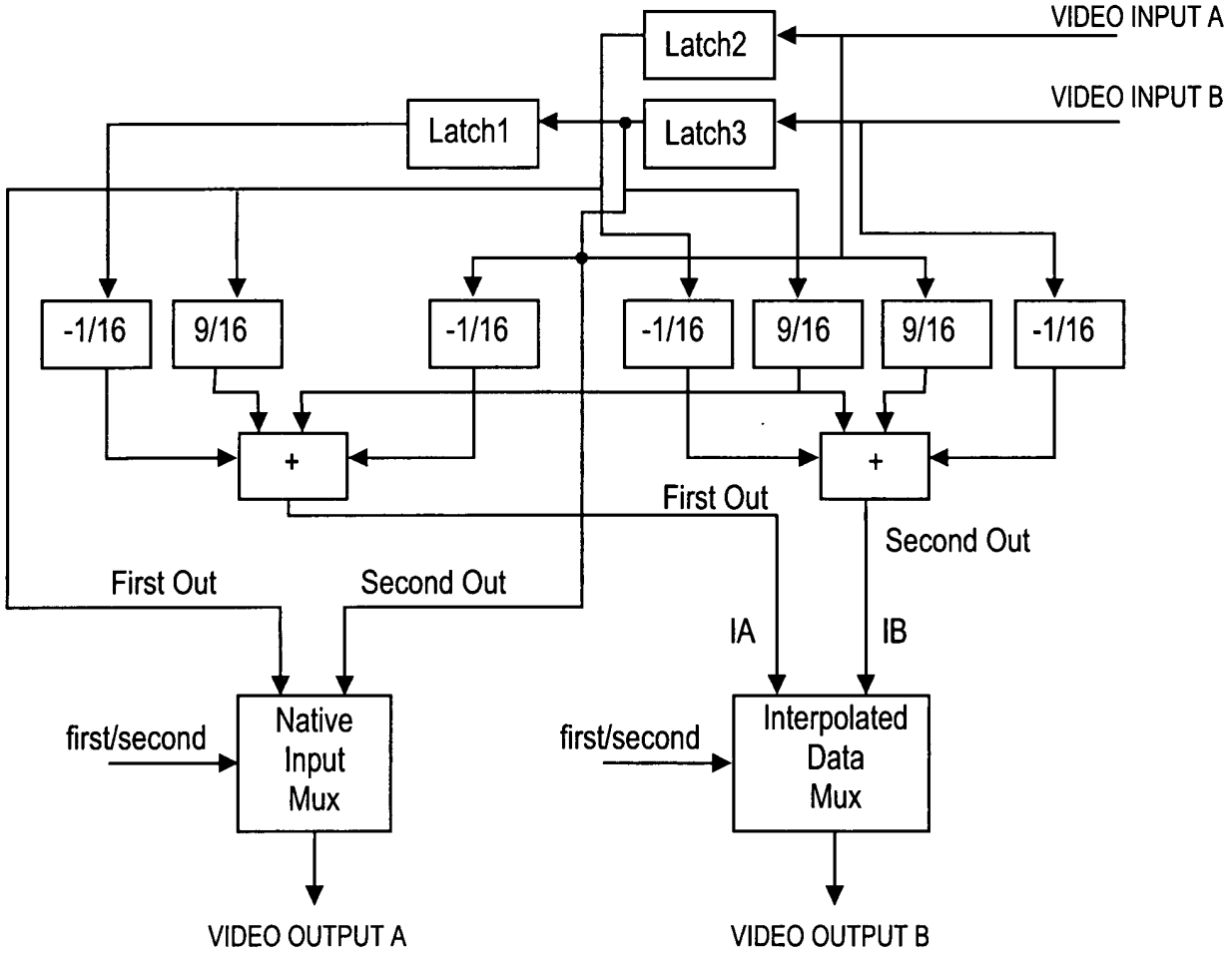
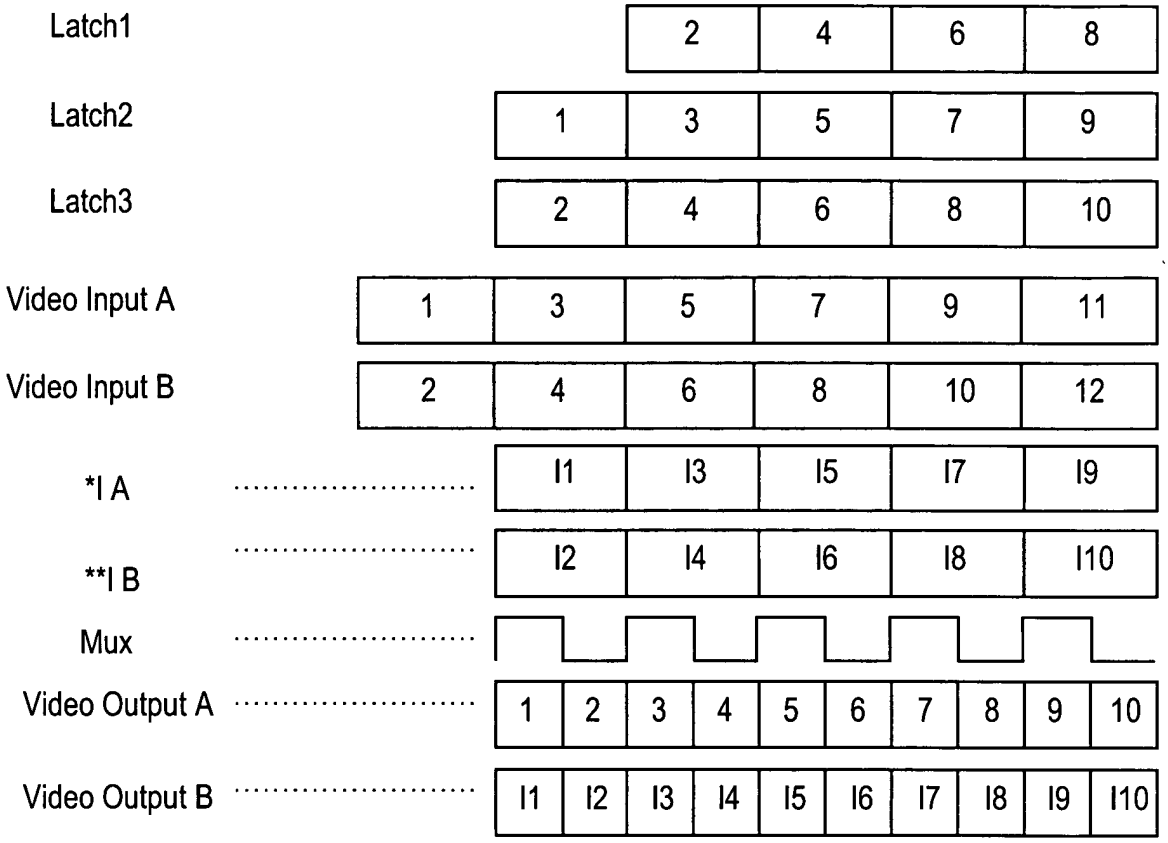

VIDEO INPUT A
VIDEO INPUT B
Latch2
Latch1
Latch3
-1/16
9/16
-1/16
-1/16
9/16
9/16
-1/16
+
+
First Out
Second Out
First Out
Second Out
IA
IB
first/second
Native Input Mux
first/second
Interpolated Data Mux
VIDEO OUTPUT A
VIDEO OUTPUT B

FIG. 32



* IA =Latch1*(-1/16) + Latch2*(9/16) + Latch3*(9/16) + Video Input A *(-1/16)

** IB =Latch2*(-1/16) + Latch3*(9/16) + Video Input A *(9/16) + Video Input A *(-1/16)

FIG. 33

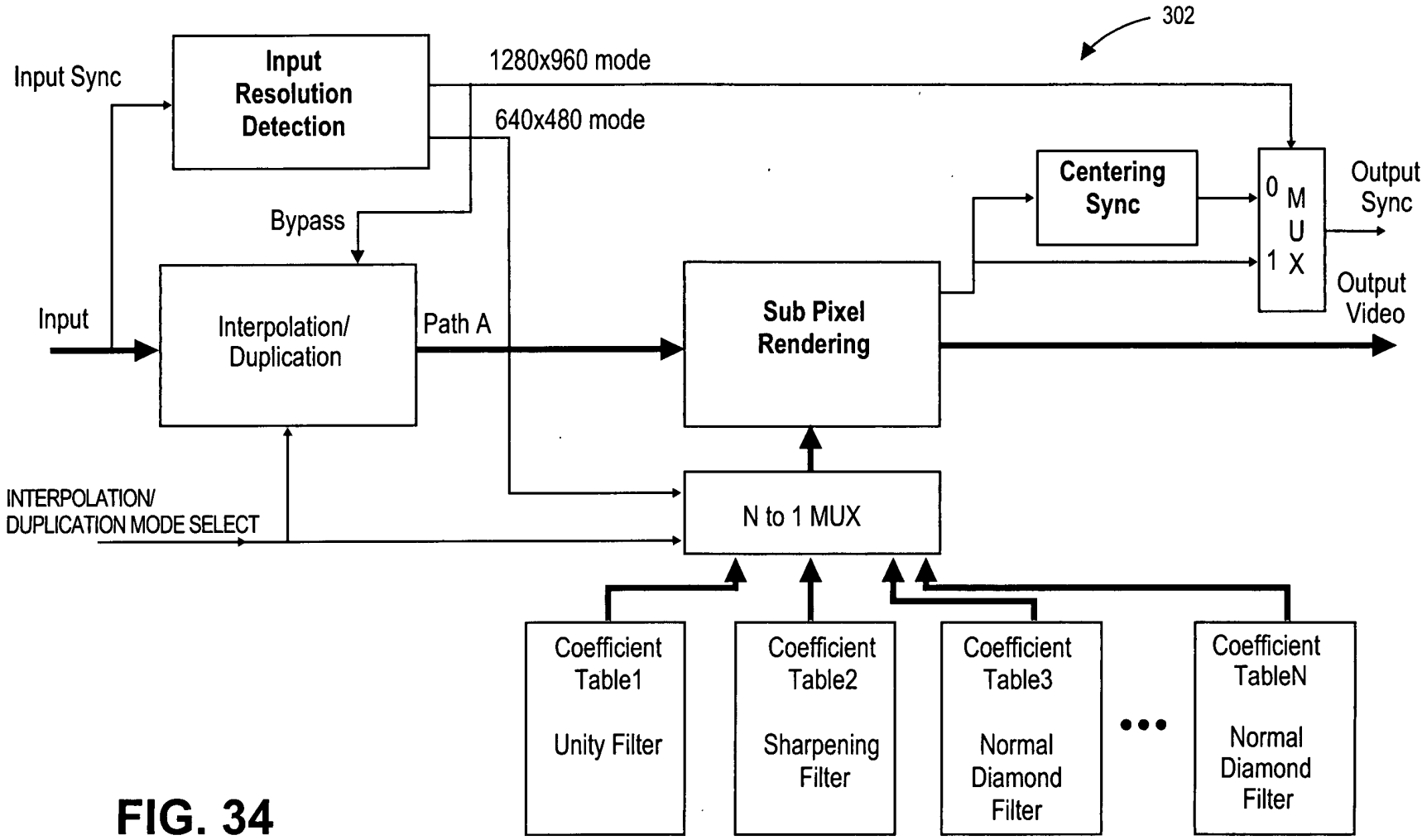

302
Input Sync
Input Resolution Detection
1280x960 mode
640x480 mode
Bypass
Input
Interpolation/ Duplication
Path A
Sub Pixel Rendering
Centering Sync
0
1
M U X
Output Sync
Output Video
INTERPOLATION/ DUPLICATION MODE SELECT
N to 1 MUX
Coefficient Table1
Unity Filter
Coefficient Table2
Sharpening Filter
Coefficient Table3
Normal Diamond Filter
Coefficient TableN
Normal Diamond Filter

FIG. 34

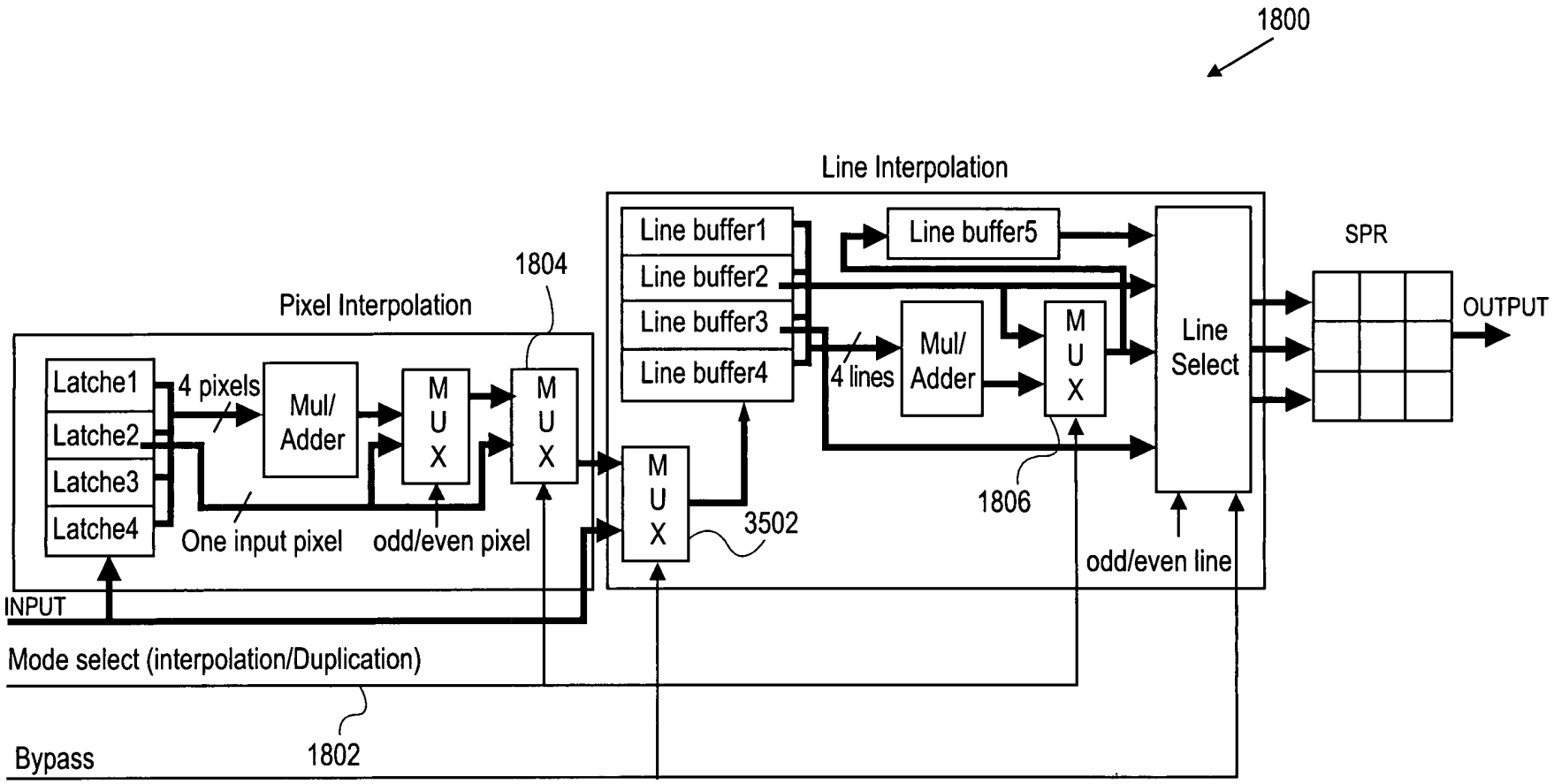

1800
Line Interpolation
Line buffer1
Line buffer2
Line buffer3
Line buffer4
Line buffer5
SPR
OUTPUT
1804
Pixel Interpolation
Latche1
Latche2
Latche3
Latche4
4 pixels
Mul/
Adder
M
U
X
4 lines
Line
Select
One input pixel
odd/even pixel
3502
1806
odd/even line
INPUT
Mode select (interpolation/Duplication)
1802
Bypass

FIG. 35

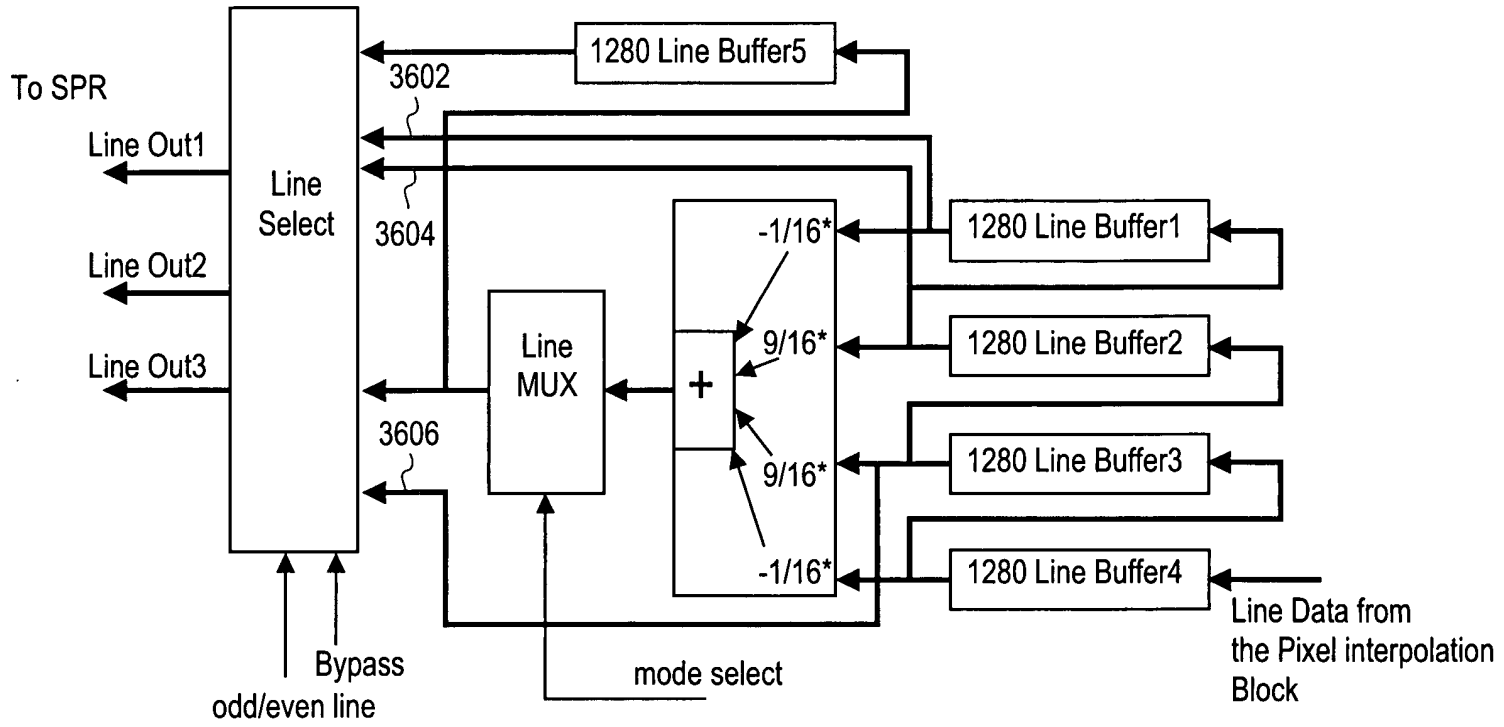
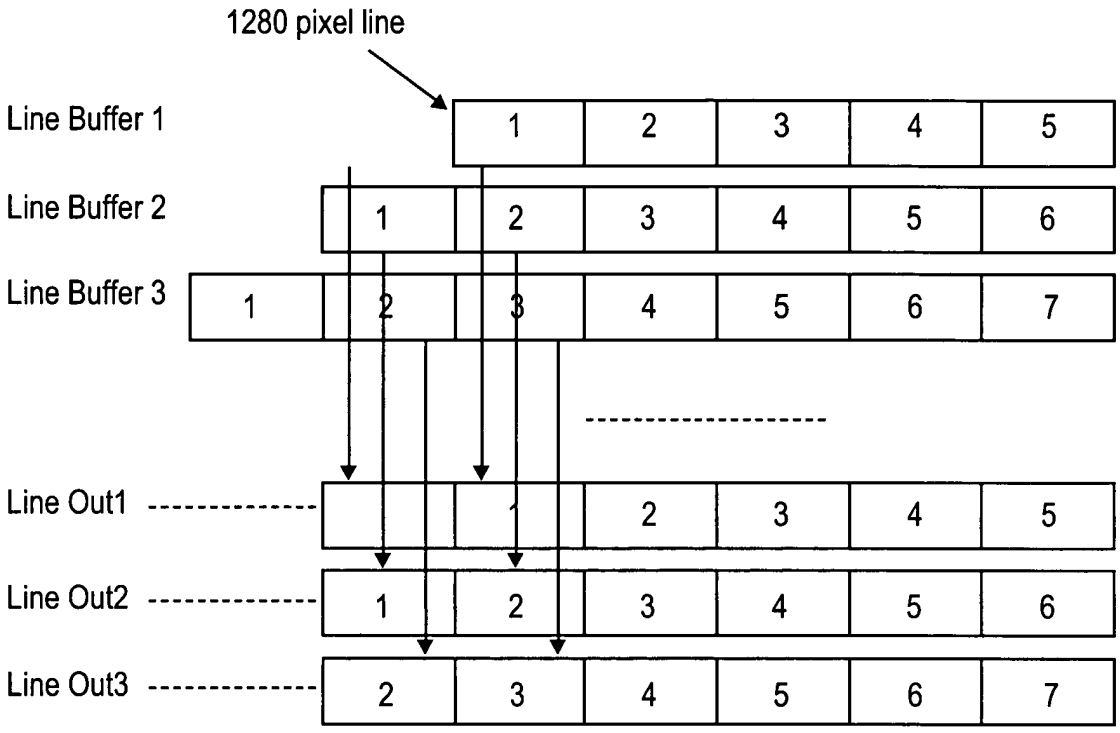

To SPR
Line Out1
Line Out2
Line Out3
Line Select
3602
3604
3606
1280 Line Buffer5
1280 Line Buffer1
1280 Line Buffer2
1280 Line Buffer3
1280 Line Buffer4
Line MUX
+
-1/16*
9/16*
9/16*
-1/16*
Bypass
odd/even line
mode select
Line Data from
the Pixel interpolation
Block

FIG. 36



Line Select Output for bypass mode

FIG. 37

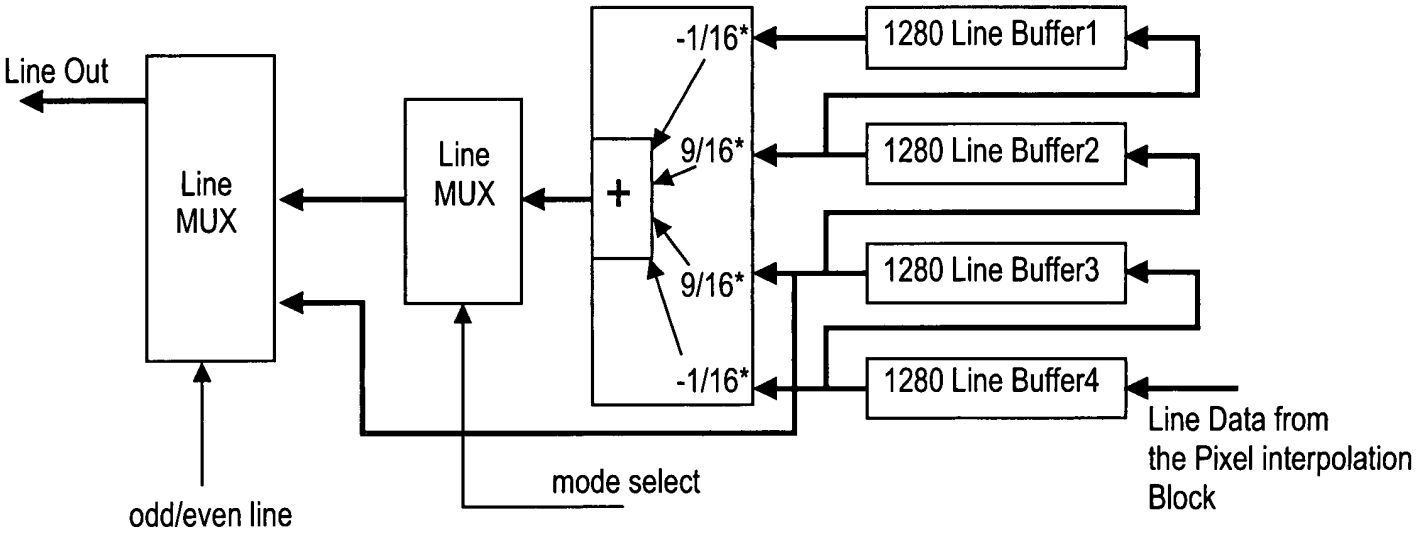

Line Out
Line MUX
Line MUX
+
-1/16*
9/16*
9/16*
-1/16*
1280 Line Buffer1
1280 Line Buffer2
1280 Line Buffer3
1280 Line Buffer4
Line Data from the Pixel interpolation Block
odd/even line
mode select

FIG. 38

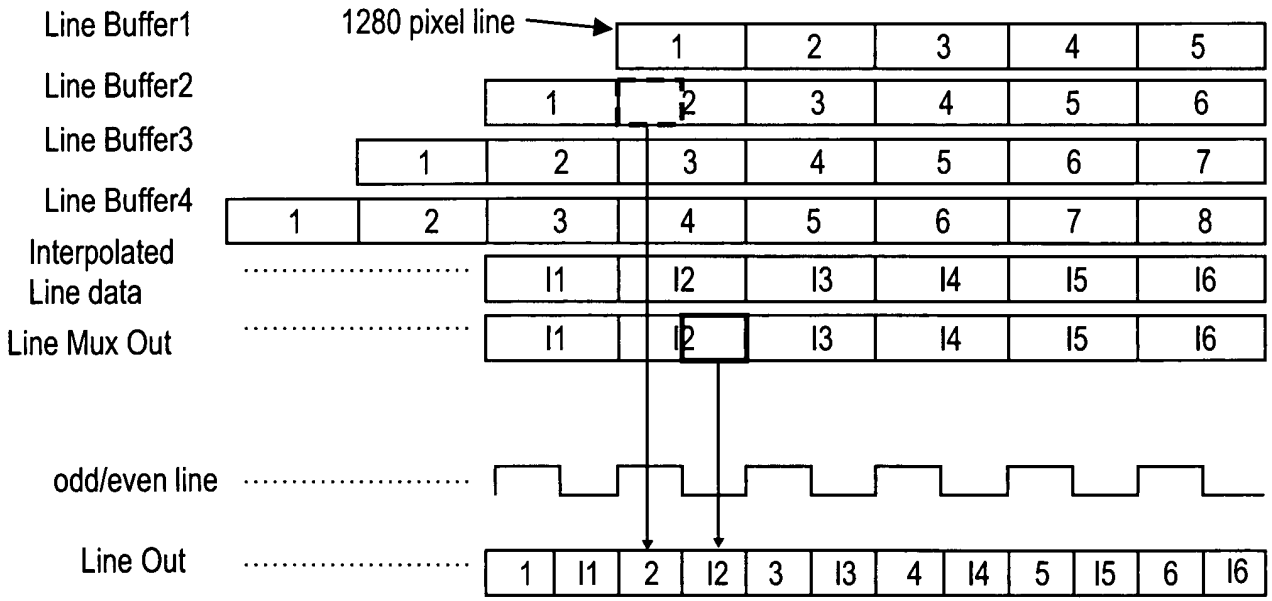

Line Buffer1
1280 pixel line
1
2
3
4
5
Line Buffer2
1
2
3
4
5
6
Line Buffer3
1
2
3
4
5
6
7
Line Buffer4
1
2
3
4
5
6
7
8
Interpolated
Line data
I1
I2
I3
I4
I5
I6
Line Mux Out
I1
I2
I3
I4
I5
I6
odd/even line
Line Out
1
I1
2
I2
3
I3
4
I4
5
I5
6
I6

FIG. 39

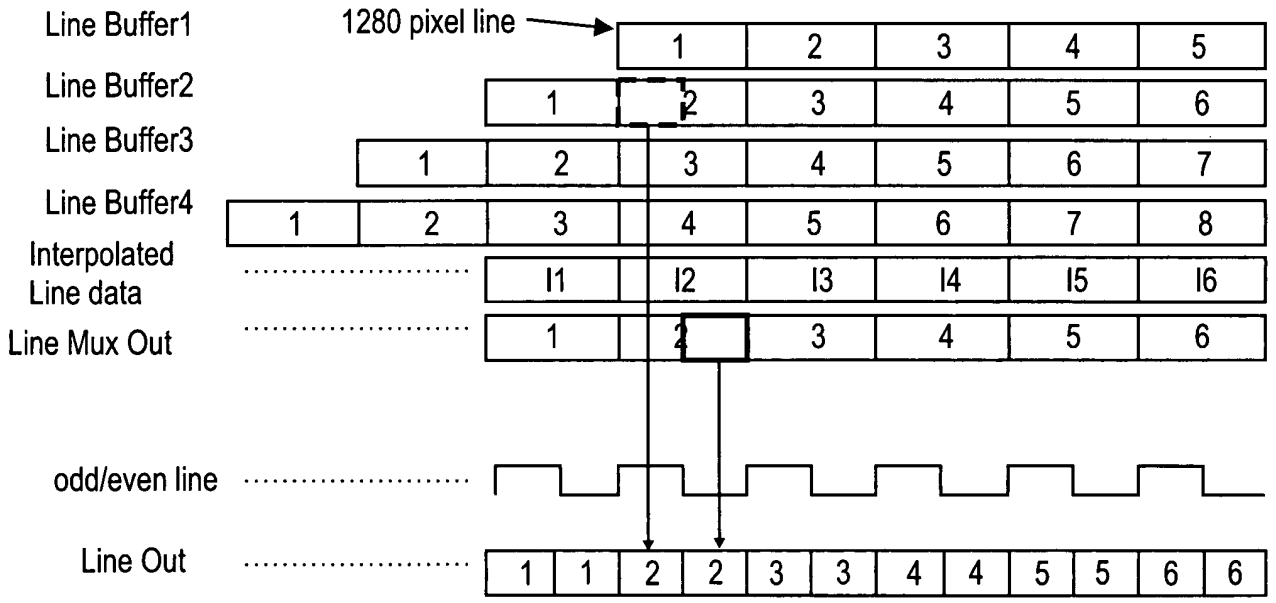

Line Buffer1
1280 pixel line
1 2 3 4 5
Line Buffer2
1 2 3 4 5 6
Line Buffer3
1 2 3 4 5 6 7
Line Buffer4
1 2 3 4 5 6 7 8
Interpolated Line data
I1 I2 I3 I4 I5 I6
Line Mux Out
1 2 3 4 5 6
odd/even line
Line Out
1 1 2 2 3 3 4 4 5 5 6 6

FIG. 40